

Soyuz 2.0 SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 32

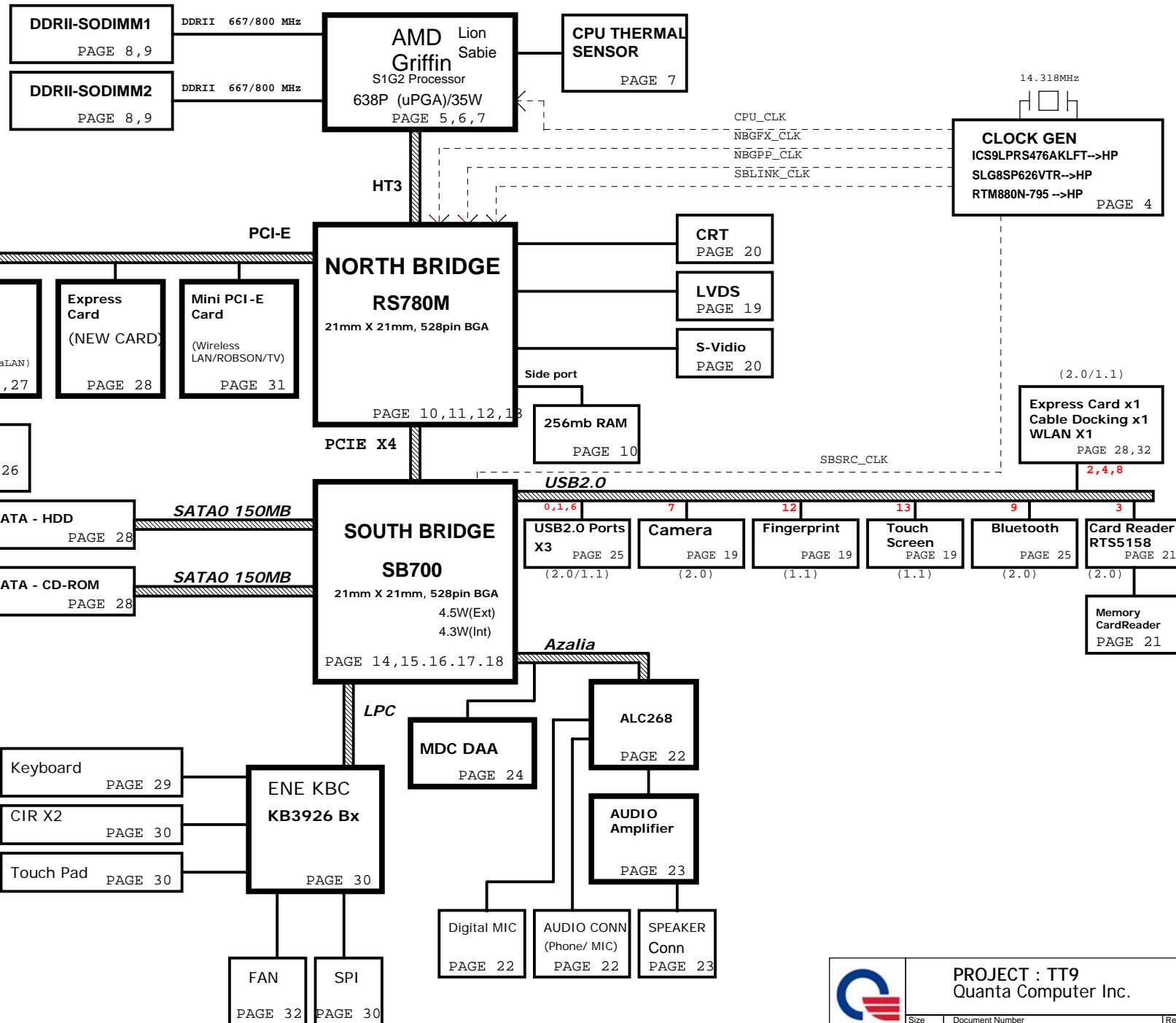
SYSTEM CHARGER(ISL6251A)
PAGE 39

SYSTEM POWER MAX1631A
PAGE 33

DDR II SMDDR_VTERM
1.8V/1.8VSUS
PAGE 36

VCCP +1.1V AND +1.2V(RT8204)
PAGE 34


CPU CORE ISL6255A
PAGE 35



Pg#	Description	NOTE
1	Schematic Block Diagram	
2	System Information	
3	Power sequence chart	
4	CLOCL GENERATOR	
5-7	AMD CPU S1G2 Griffin	
8-9	DDR II SO-DIMM	
10-13	RS780M	
14-18	SB700	
19	LCD CONNECTOR / LCD PWR / LID	
20	20--CRT,TV_OUT	
21	RTS5158E & CR SOCKET	
22	Azalia ALC268	
23	JACK/AMP_TPA0312	
24	Si3080 and MDC1.5 Connector	
25	Blue Tooth / USBX3 / TPM	
26	RTL8111C/RJ45	
27	LAN Power	
28	NEW CARD/SATA ODD/SATA HDD	
29	LED/KEYBOARD/SW	
30	KB3926/ROM/TP	
31	Mini CARD/Hole	
32	CABLE DOCKING/FAN	
33	3V/5V(MAX1631A)	
34	+1.2V/+1.1V (RT8204)	
35	+CPU_CORE ISL6265	
36	+1.8VSUS/+1.8V/+2.5V	
37	+1.1V/+1.2V_S5/+1.5V	
38	DISCHARGE	
39	Charger (ISL6251)	

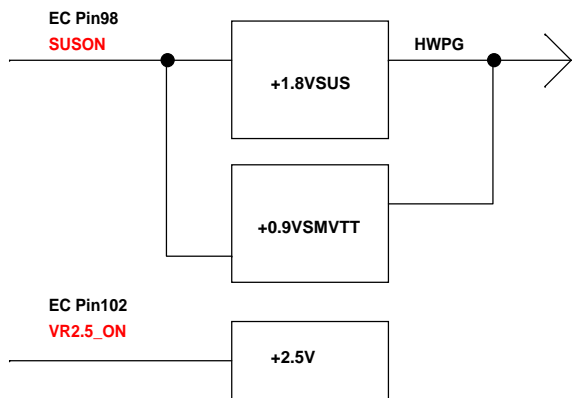
* --> Un-stuff (ex. *1K/04)
 04-- 0402 footprint
 06-- 0603 footprint
 08-- 0805 footprint
 12-- 1206 footprint
 F-- 1% tolerance

Power & Ground

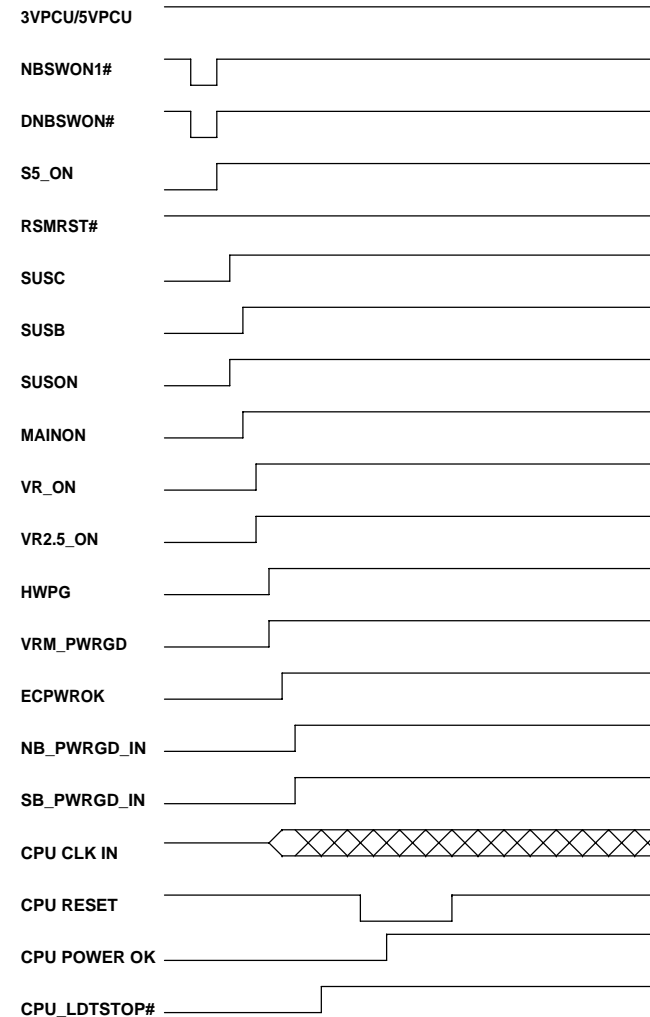
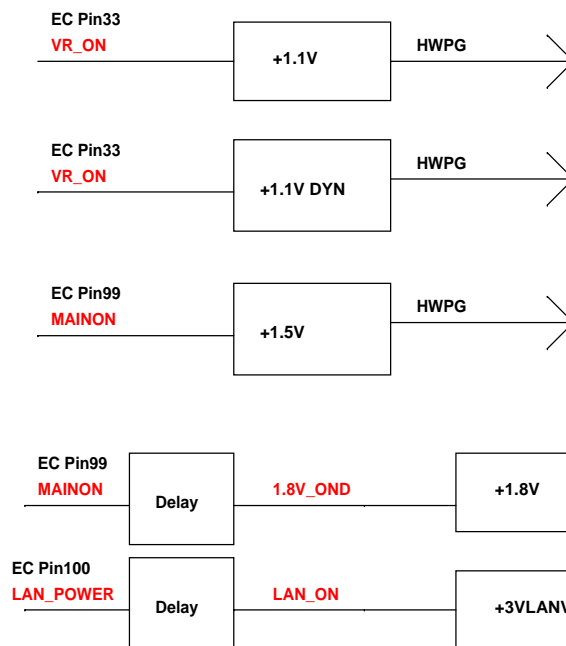
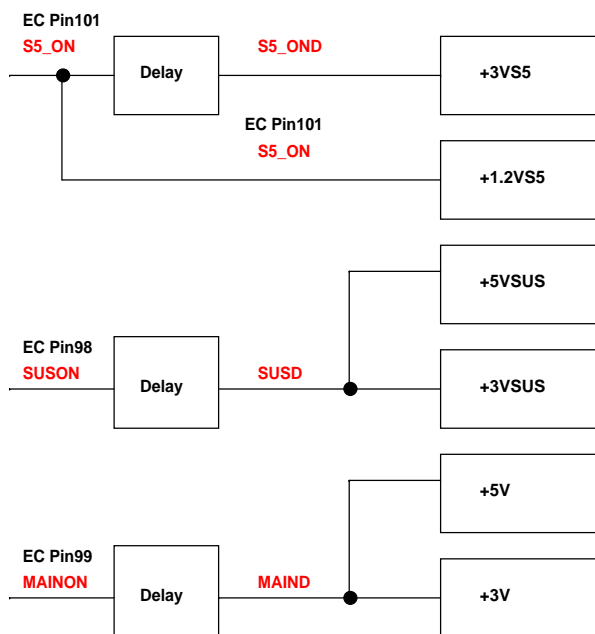
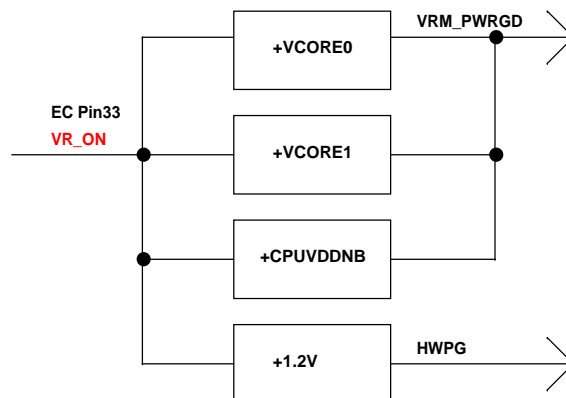
Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (18.5V)	
+BATT	S0, S3, S4, S5	MAIN BATTERY + (6.2V-8.4V)	
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3.3V)	
+12VALW	S0, S3, S4, S5	+12V	
+VCORE	S0	CPU CORE POWER (0.375-1.5V)	VRON
+CPUVDDNB	S0	CPU CORE POWER (1.375-1.5V)	VRON
+1.1V_NB	S0	+1.1 to +1.0 DYN	VRON
+1.1V	S0	+1.1V	VRON
+1.2VS5	S0, S3, S4, S5		S5_ON
+1.2V	S0	+1.2V	VRON
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
+5VSUS	S0, S3		SUSON
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+1.8V	S0		MAINON
+2.5V	S0	CPU VDDA	VR2.5_ON
+0.9VSMVTT	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
+0.9VSMVREF_DIMM	S0, S3	DDR REF POWER	SUSON
+AVDD	S0	AUDIO ANALOG POWER (5V)	MAINON
+3VLAVCC	S0, S3, S4, S5	LAN Power	LAN_ON
 GND	ALL PAGES	DIGITAL GROUND	
 AGND		AUDIO GND	

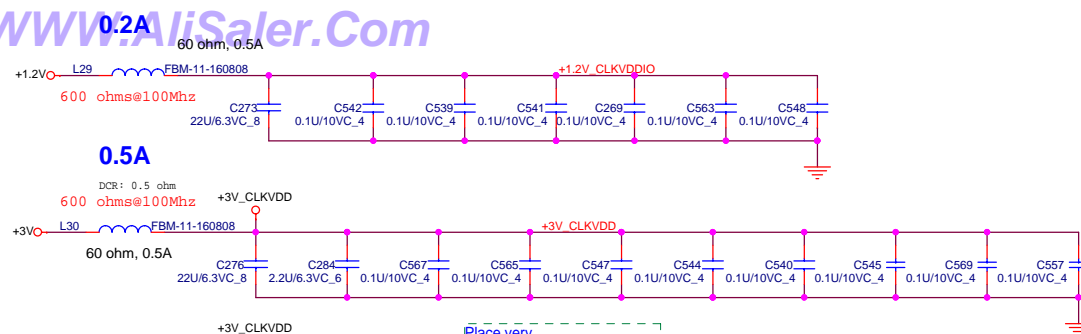
SMBUS	SMBUS function define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card (+3VS5)
SMBCLK2 SMBDAT2	New CARD (+3VS5)

CPU Power Group A



CPU Power Group B

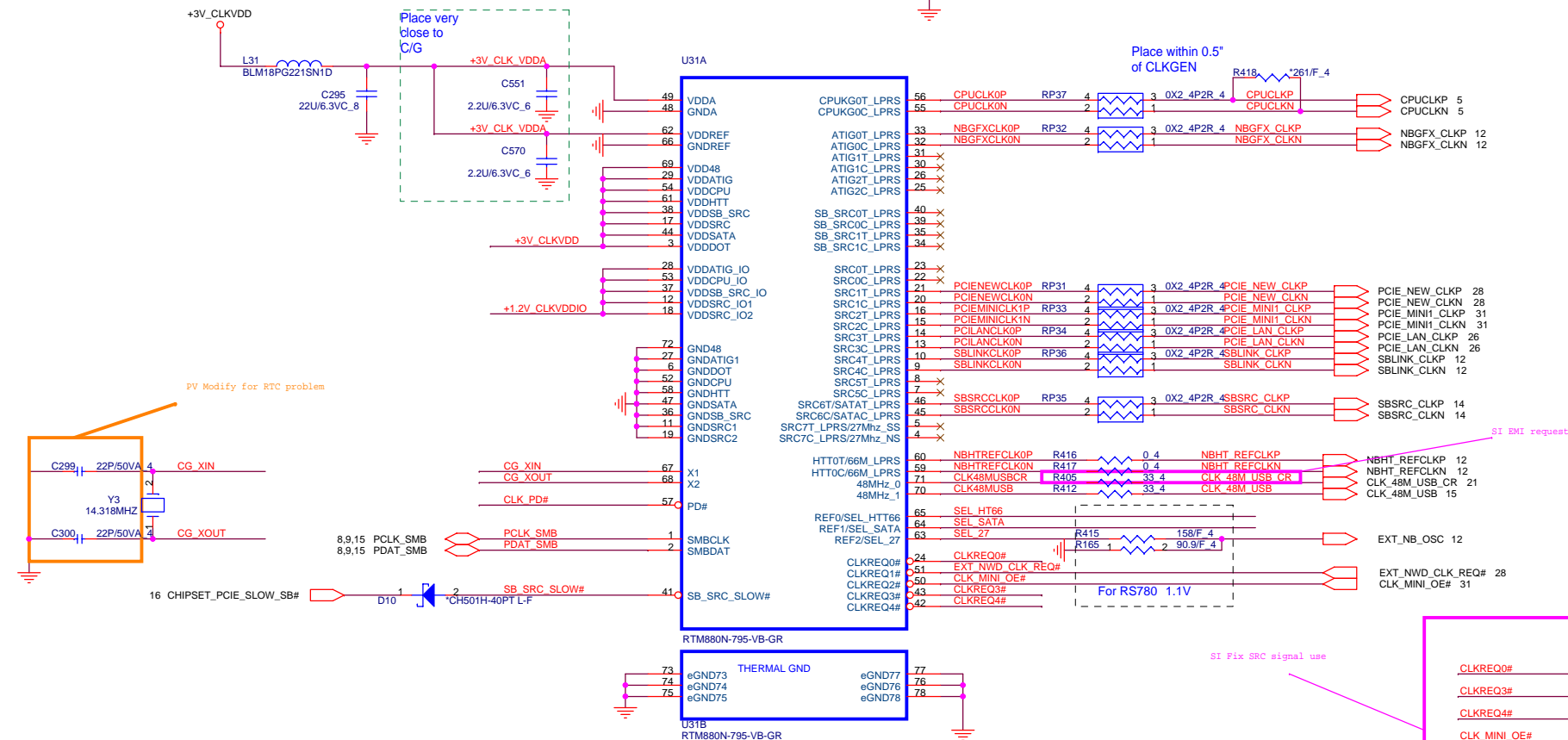




Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

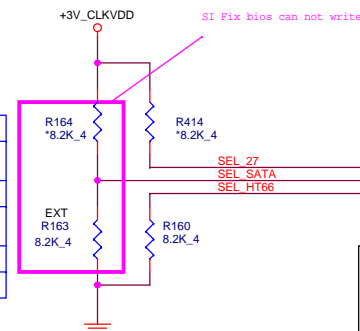


when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

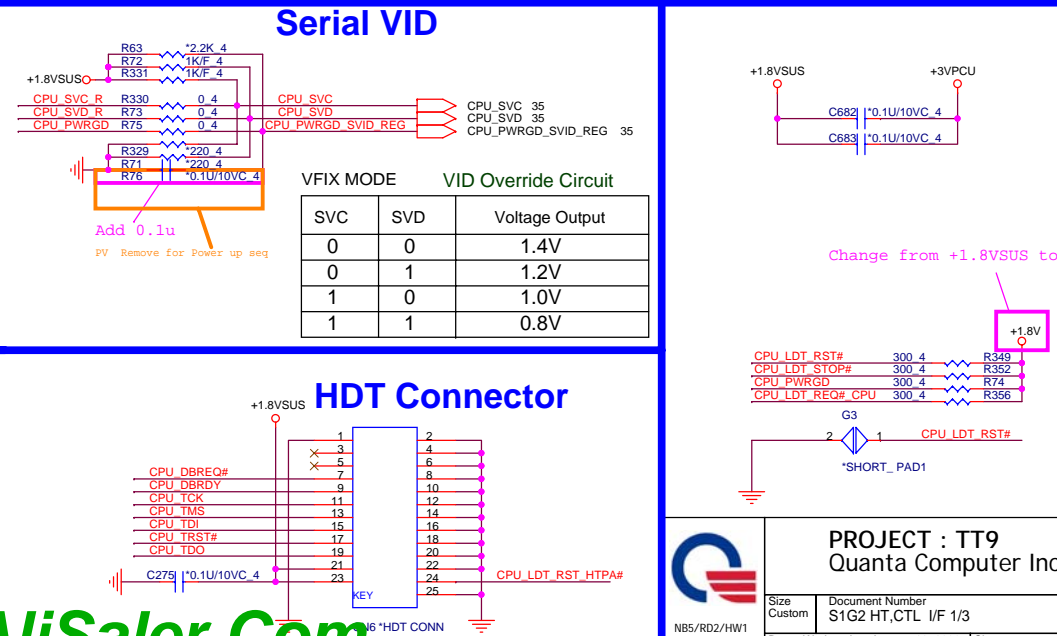
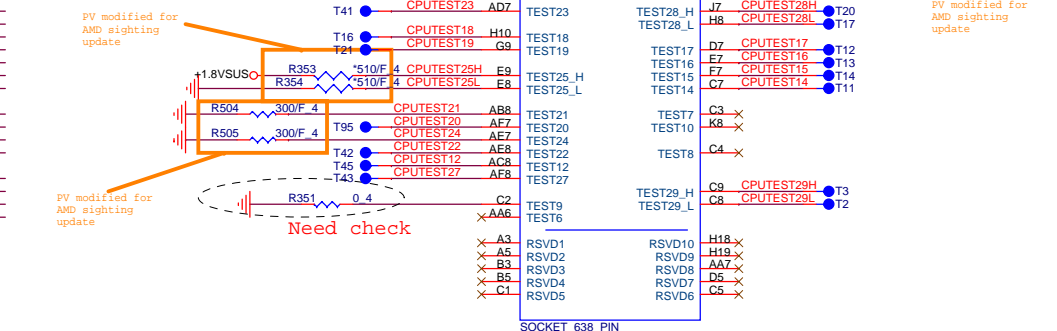
* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	0	100 MHz spreading differential SRC clock
	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

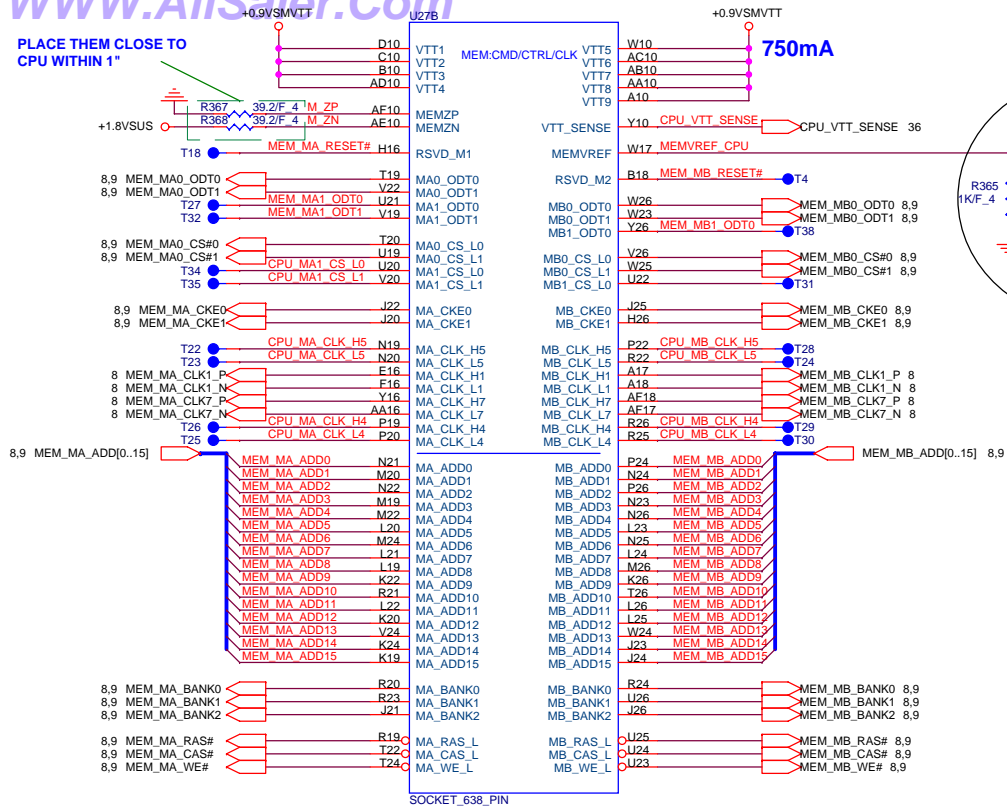


PROJECT : TT9
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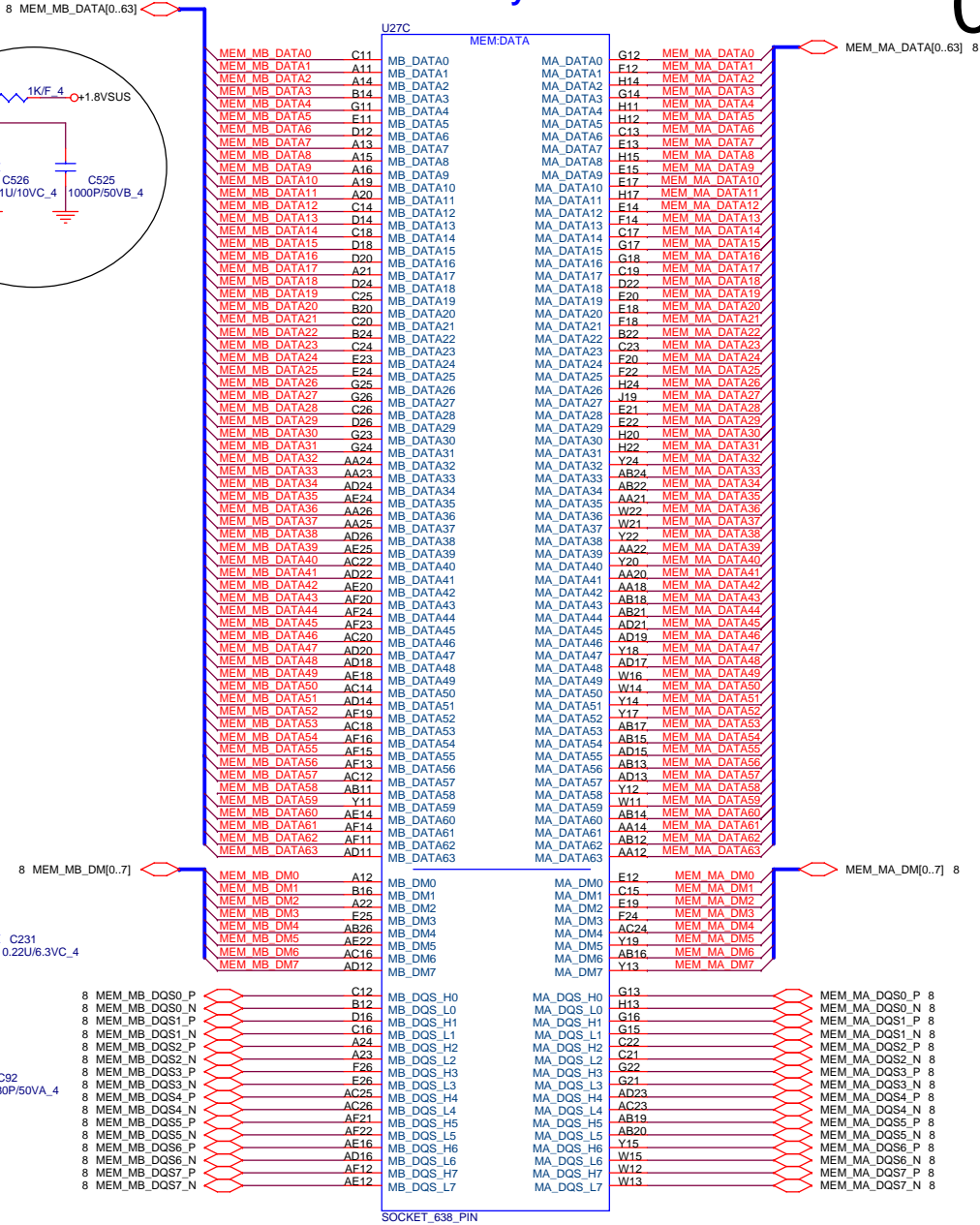
Size Custom	Document Number Clock generator	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 4 of 41	



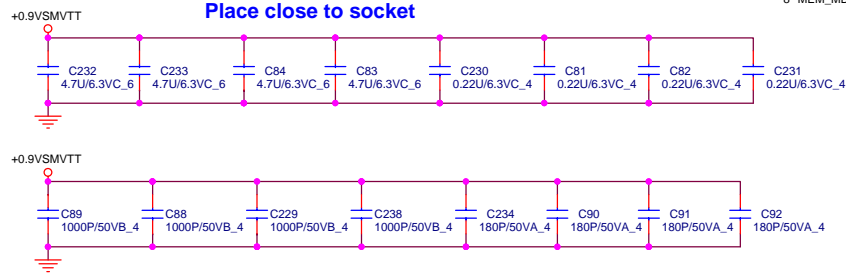
PLACE THEM CLOSE TO CPU WITHIN 1"



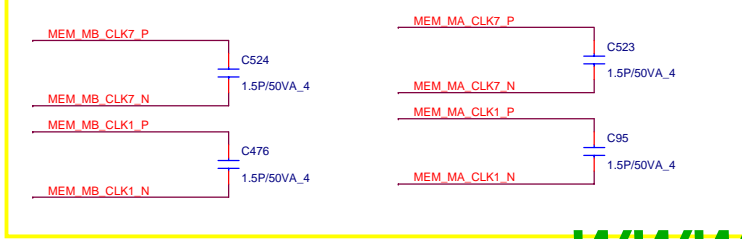
Processor Memory Interface



Place close to socket



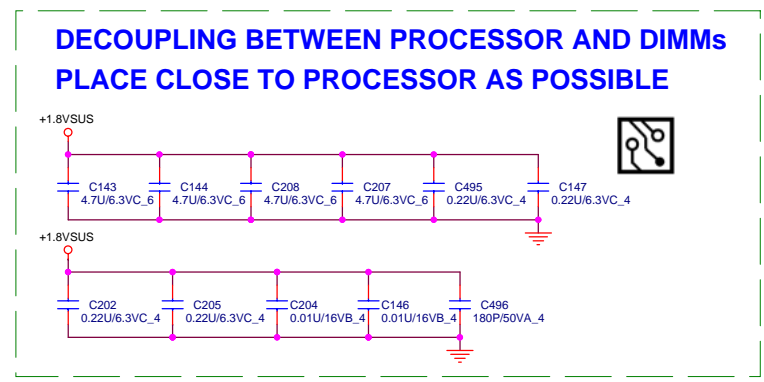
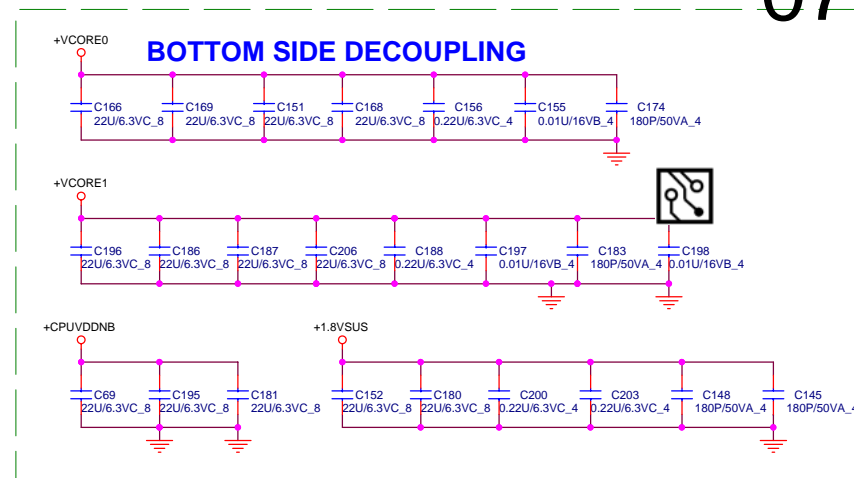
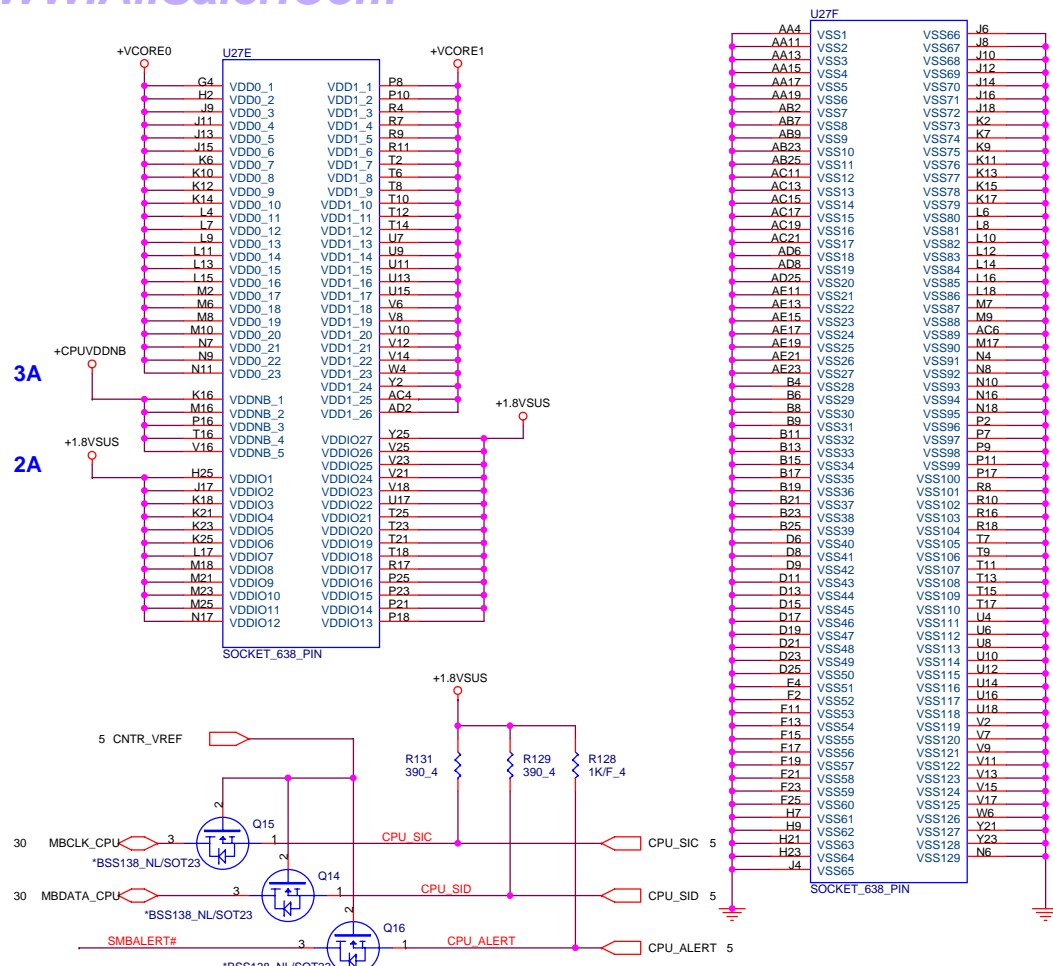
Close to CPU within 1500 mils



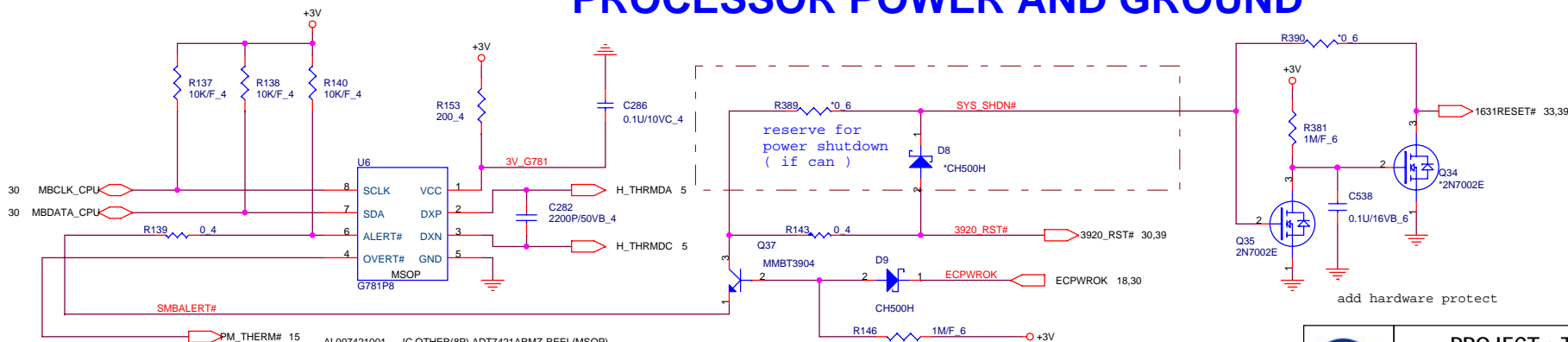
+0.9VSMVTT 9.31,36
+1.8VVSUS 5.7,8,9,31,35,36,37



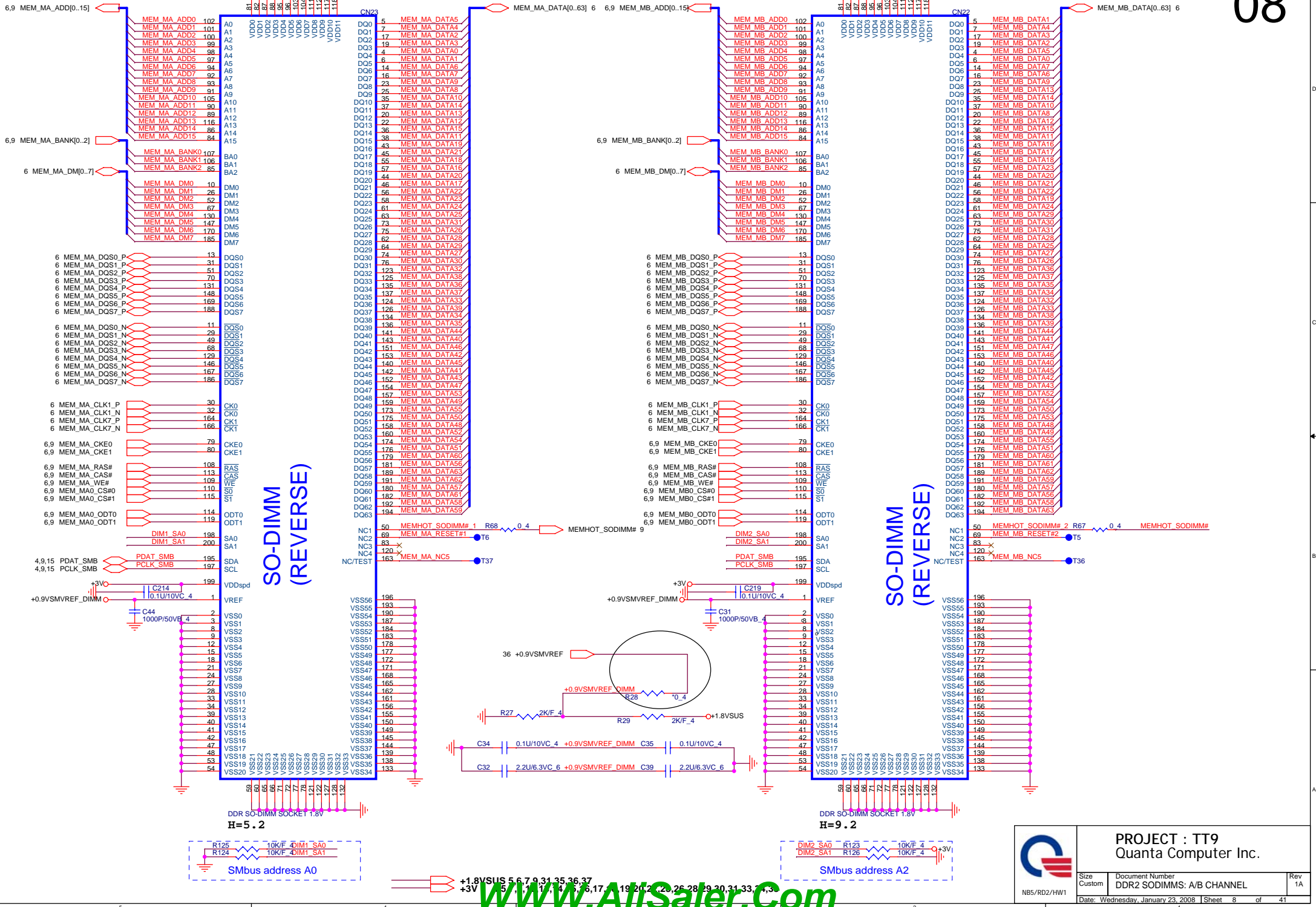
PROJECT : TT9
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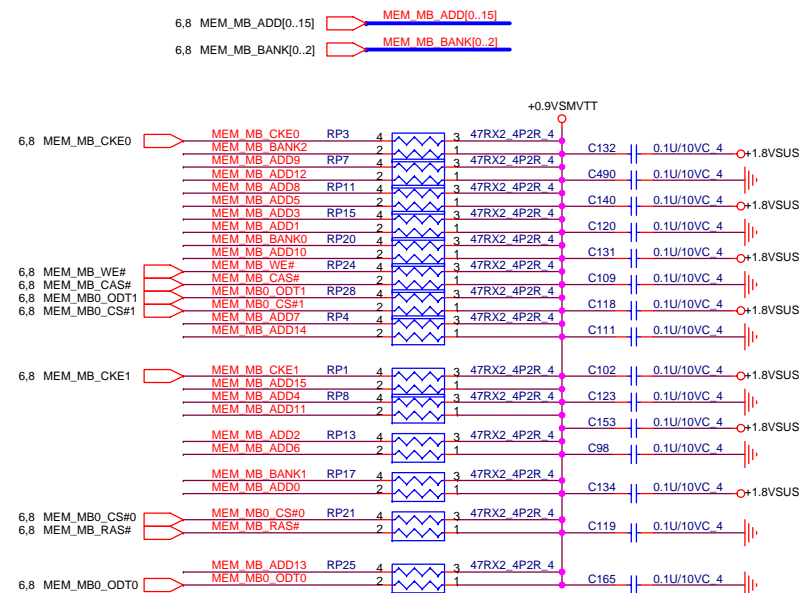
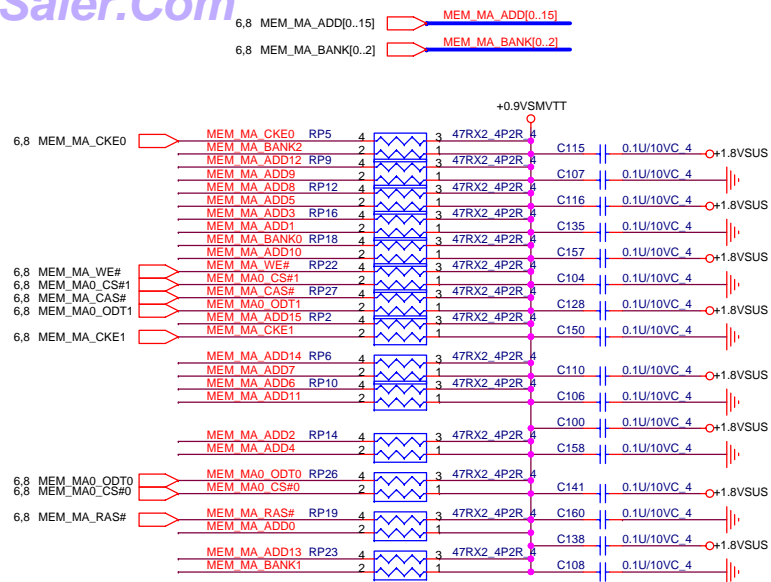


PROCESSOR POWER AND GROUND

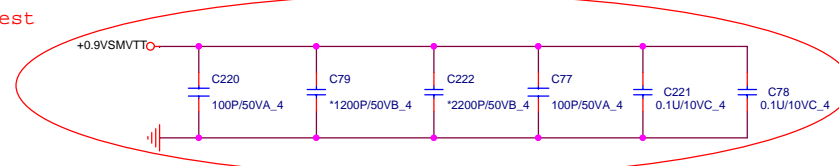


+VCORE0 35
 +VCORE1 35
 +CPUVDDNB 35
 +1.8VSUS 5,6,8,9,31,35,36,37
 +1.8VSUS 4,5,9,12,13,14,15,16,18,19,20,22,23,26,28,29,30,31,33,34,38





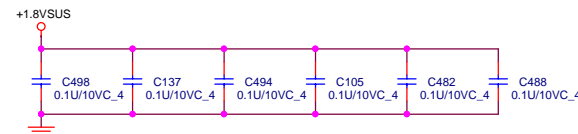
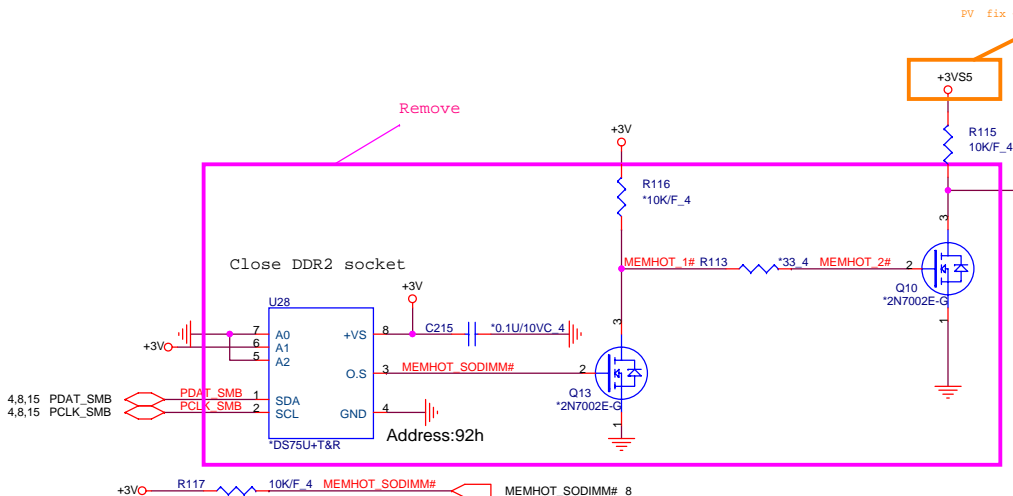
Emi request



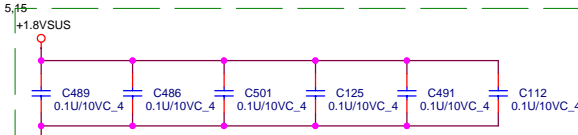
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO SOCKET(PER EMI/EMC)



PLACE CLOSE TO SOCKET(PER EMI/EMC)



PROJECT : TT9
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Size Custom	Document Number	Rev 1A
DBS/RD2/HW1	DDR2 SODIMMS TERMINATIONS	
Date: Wednesday, January 23, 2008	Sheet 9 of 41	

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CPU_NB_CAD_H0 Y25 HT_RXCAD0P
HT_CPU_NB_CAD_L0 Y24 HT_TXCAD0N
HT_CPU_NB_CAD_H1 V22 HT_RXCAD1P
HT_CPU_NB_CAD_L1 V23 HT_TXCAD1N
HT_CPU_NB_CAD_H2 V25 HT_RXCAD2P
HT_CPU_NB_CAD_L2 V24 HT_TXCAD2N
HT_CPU_NB_CAD_H3 U24 HT_RXCAD3P
HT_CPU_NB_CAD_L3 U25 HT_TXCAD3N
HT_CPU_NB_CAD_H4 T25 HT_RXCAD4P
HT_CPU_NB_CAD_L4 T24 HT_TXCAD4N
HT_CPU_NB_CAD_H5 P22 HT_RXCAD5P
HT_CPU_NB_CAD_L5 P23 HT_TXCAD5N
HT_CPU_NB_CAD_H6 P25 HT_RXCAD6P
HT_CPU_NB_CAD_L6 P24 HT_TXCAD6N
HT_CPU_NB_CAD_H7 N24 HT_RXCAD7P
HT_CPU_NB_CAD_L7 N25 HT_TXCAD7N

HT_CPU_NB_CAD_H8 AC24 HT_RXCAD8P
HT_CPU_NB_CAD_L8 AC25 HT_TXCAD8N
HT_CPU_NB_CAD_H9 AB25 HT_RXCAD9P
HT_CPU_NB_CAD_L9 AB24 HT_TXCAD9N
HT_CPU_NB_CAD_H10 AA24 HT_RXCAD10P
HT_CPU_NB_CAD_L10 AA25 HT_TXCAD10N
HT_CPU_NB_CAD_H11 Y22 HT_RXCAD11P
HT_CPU_NB_CAD_L11 Y23 HT_TXCAD11N
HT_CPU_NB_CAD_H12 W21 HT_RXCAD12P
HT_CPU_NB_CAD_L12 W20 HT_TXCAD12N
HT_CPU_NB_CAD_H13 V21 HT_RXCAD13P
HT_CPU_NB_CAD_L13 V20 HT_TXCAD13N
HT_CPU_NB_CAD_H14 U20 HT_RXCAD14P
HT_CPU_NB_CAD_L14 U21 HT_TXCAD14N
HT_CPU_NB_CAD_H15 U19 HT_RXCAD15P
HT_CPU_NB_CAD_L15 U18 HT_TXCAD15N

HT_CPU_NB_CLK_H0 T22 HT_RXCLK0P
HT_CPU_NB_CLK_L0 T23 HT_TXCLK0N
HT_CPU_NB_CLK_H1 AB23 HT_RXCLK1P
HT_CPU_NB_CLK_L1 AA22 HT_TXCLK1N

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
HT_CPU_NB_CTL_L0 M23 HT_TXCTL0N
HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
HT_CPU_NB_CTL_L1 R20 HT_TXCTL1N

HT_RXCALP C23 HT_TXCALP
HT_RXCALN A24 HT_TXCALN

HT_NB_CPU_CAD_H0 D24 HT_RXCAD0P
HT_NB_CPU_CAD_L0 D25 HT_TXCAD0N
HT_NB_CPU_CAD_H1 E24 HT_RXCAD1P
HT_NB_CPU_CAD_L1 E25 HT_TXCAD1N
HT_NB_CPU_CAD_H2 F24 HT_RXCAD2P
HT_NB_CPU_CAD_L2 F25 HT_TXCAD2N
HT_NB_CPU_CAD_H3 F23 HT_RXCAD3P
HT_NB_CPU_CAD_L3 F22 HT_TXCAD3N
HT_NB_CPU_CAD_H4 H23 HT_RXCAD4P
HT_NB_CPU_CAD_L4 H22 HT_TXCAD4N
HT_NB_CPU_CAD_H5 J25 HT_RXCAD5P
HT_NB_CPU_CAD_L5 J24 HT_TXCAD5N
HT_NB_CPU_CAD_H6 K24 HT_RXCAD6P
HT_NB_CPU_CAD_L6 K25 HT_TXCAD6N
HT_NB_CPU_CAD_H7 K23 HT_RXCAD7P
HT_NB_CPU_CAD_L7 K22 HT_TXCAD7N

HT_NB_CPU_CAD_H8 F21 HT_RXCAD8P
HT_NB_CPU_CAD_L8 G21 HT_TXCAD8N
HT_NB_CPU_CAD_H9 G20 HT_RXCAD9P
HT_NB_CPU_CAD_L9 H21 HT_TXCAD9N
HT_NB_CPU_CAD_H10 J21 HT_RXCAD10P
HT_NB_CPU_CAD_L10 J21 HT_TXCAD10N
HT_NB_CPU_CAD_H11 J18 HT_RXCAD11P
HT_NB_CPU_CAD_L11 K17 HT_TXCAD11N
HT_NB_CPU_CAD_H12 L19 HT_RXCAD12P
HT_NB_CPU_CAD_L12 L18 HT_TXCAD12N
HT_NB_CPU_CAD_H13 M19 HT_RXCAD13P
HT_NB_CPU_CAD_L13 L18 HT_TXCAD13N
HT_NB_CPU_CAD_H14 M21 HT_RXCAD14P
HT_NB_CPU_CAD_L14 P21 HT_TXCAD14N
HT_NB_CPU_CAD_H15 P18 HT_RXCAD15P
HT_NB_CPU_CAD_L15 M18 HT_TXCAD15N

HT_NB_CPU_CLK_H0 H24 HT_RXCLK0P
HT_NB_CPU_CLK_L0 H25 HT_TXCLK0N
HT_NB_CPU_CLK_H1 L21 HT_RXCLK1P
HT_NB_CPU_CLK_L1 L20 HT_TXCLK1N

HT_NB_CPU_CTL_H0 M24 HT_RXCTL0P
HT_NB_CPU_CTL_L0 M25 HT_TXCTL0N
HT_NB_CPU_CTL_H1 P19 HT_RXCTL1P
HT_NB_CPU_CTL_L1 P18 HT_TXCTL1N

HT_TXCALP B24 HT_TXCALN
HT_TXCALN B25 HT_TXCALP

PV modified --
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

PV modified --
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

PAR 4 OF 6

SBD_MEM/DVO_I/F

SPM_A0 AB12 MEM_A0(NC)
SPM_A1 AE16 MEM_A1(NC)
SPM_A2 V11 MEM_A2(NC)
SPM_A3 AE15 MEM_A3(NC)
SPM_A4 AA12 MEM_A4(NC)
SPM_A5 AB16 MEM_A5(NC)
SPM_A6 AB14 MEM_A6(NC)
SPM_A7 AD14 MEM_A7(NC)
SPM_A8 AD13 MEM_A8(NC)
SPM_A9 AD15 MEM_A9(NC)
SPM_A10 AC16 MEM_A10(NC)
SPM_A11 AC13 MEM_A11(NC)
SPM_A12 AC14 MEM_A12(NC)
SPM_A13 Y14 MEM_A13(NC)

SPM_BA0 AD16 MEM_BA0(NC)
SPM_BA1 AE17 MEM_BA1(NC)
SPM_BA2 AD17 MEM_BA2(NC)

SPM_RAS# Y12C MEM_RASb(NC)
SPM_CAS# Y12C MEM_CASb(NC)
SPM_WE# AD18C MEM_Web(NC)
SPM_CS# AB13C MEM_Csb(NC)
SPM_CKE AB18C MEM_CKE(NC)
SPM_ODT V14C MEM_ODT(NC)

SPM_CLKP W15C MEM_CKp(NC)
SPM_CLKN W14C MEM_CK(NC)

MEM_DQ0/DVO_VSYNc(NC) AA18 SPM_DQ0
MEM_DQ1/DVO_HSYNc(NC) AA20 SPM_DQ1
MEM_DQ2/DVO_DE(NC) AA19 SPM_DQ2
MEM_DQ3/DVO_D0(NC) V19 SPM_DQ3
MEM_DQ4(NC) V17 SPM_DQ4
MEM_DQ5/DVO_D1(NC) AA17 SPM_DQ5
MEM_DQ6/DVO_D2(NC) AA15 SPM_DQ6
MEM_DQ7/DVO_D4(NC) Y15 SPM_DQ7
MEM_DQ8/DVO_D3(NC) AC20 SPM_DQ8
MEM_DQ9/DVO_D5(NC) AD19 SPM_DQ9
MEM_DQ10/DVO_D6(NC) AC18 SPM_DQ10
MEM_DQ11/DVO_D7(NC) AB20 SPM_DQ11
MEM_DQ12(NC) AD22 SPM_DQ12
MEM_DQ13/DVO_D9(NC) AC22 SPM_DQ13
MEM_DQ14/DVO_D10(NC) AD21 SPM_DQ14
MEM_DQ15/DVO_D11(NC) AD21 SPM_DQ15

MEM_DQS0P/DVO_IDCKP(NC) Y17 SPM_DQS0P
MEM_DQS0N/DVO_IDCKN(NC) W18 SPM_DQS0N
MEM_DQS1P(NC) AD20 SPM_DQS1P
MEM_DQS1N(NC) AE21 SPM_DQS1N

MEM_DM0(NC) W17 SPM_DM0
MEM_DM1/DVO_D8(NC) AE19 SPM_DM1

MEM_COMP(NC) AE23 SPM_VREF1
MEM_COMPN(NC) AE24 SPM_VREF1

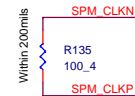
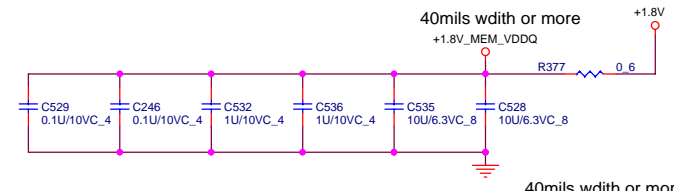
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MEM_DQ1/DVO_HSYNc(NC) AA20 SPM_DQ1
MEM_DQ2/DVO_DE(NC) AA19 SPM_DQ2
MEM_DQ3/DVO_D0(NC) V19 SPM_DQ3
MEM_DQ4(NC) V17 SPM_DQ4
MEM_DQ5/DVO_D1(NC) AA17 SPM_DQ5
MEM_DQ6/DVO_D2(NC) AA15 SPM_DQ6
MEM_DQ7/DVO_D4(NC) Y15 SPM_DQ7
MEM_DQ8/DVO_D3(NC) AC20 SPM_DQ8
MEM_DQ9/DVO_D5(NC) AD19 SPM_DQ9
MEM_DQ10/DVO_D6(NC) AC18 SPM_DQ10
MEM_DQ11/DVO_D7(NC) AB20 SPM_DQ11
MEM_DQ12(NC) AD22 SPM_DQ12
MEM_DQ13/DVO_D9(NC) AC22 SPM_DQ13
MEM_DQ14/DVO_D10(NC) AD21 SPM_DQ14
MEM_DQ15/DVO_D11(NC) AD21 SPM_DQ15

MEM_DQS0P/DVO_IDCKP(NC) Y17 SPM_DQS0P
MEM_DQS0N/DVO_IDCKN(NC) W18 SPM_DQS0N
MEM_DQS1P(NC) AD20 SPM_DQS1P
MEM_DQS1N(NC) AE21 SPM_DQS1N

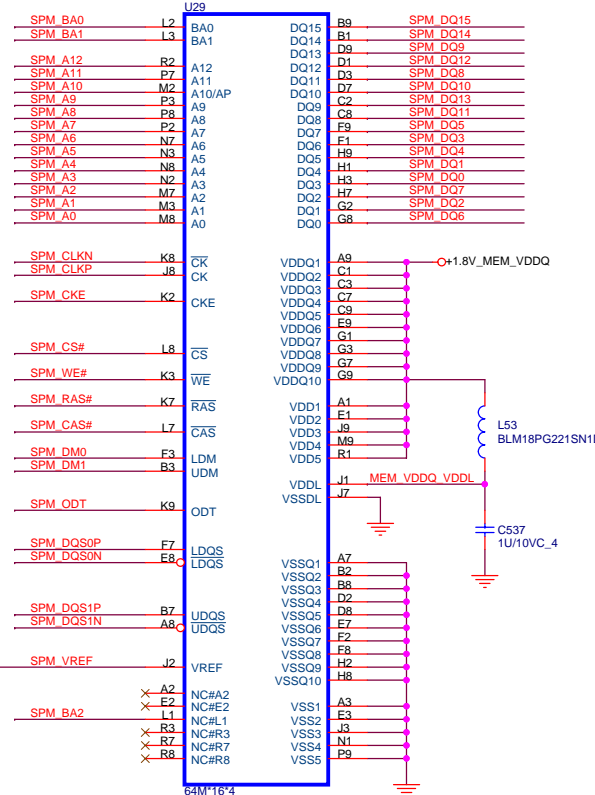
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MEM_DM1/DVO_D8(NC) AE19 SPM_DM1

MEM_COMP(NC) AE23 SPM_VREF1
MEM_COMPN(NC) AE24 SPM_VREF1

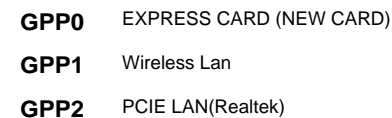
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HT_CPU_NB_CAD_L15_0 HT_CPU_NB_CAD_L15_0 5
HT_CPU_NB_CLK_H1_0 HT_CPU_NB_CLK_H1_0 5
HT_CPU_NB_CLK_L1_0 HT_CPU_NB_CLK_L1_0 5
HT_CPU_NB_CTL_H1_0 HT_CPU_NB_CTL_H1_0 5
HT_CPU_NB_CTL_L1_0 HT_CPU_NB_CTL_L1_0 5
HT_NB_CPU_CAD_H15_0 HT_NB_CPU_CAD_H15_0 5
HT_NB_CPU_CAD_L15_0 HT_NB_CPU_CAD_L15_0 5
HT_NB_CPU_CLK_H1_0 HT_NB_CPU_CLK_H1_0 5
HT_NB_CPU_CLK_L1_0 HT_NB_CPU_CLK_L1_0 5
HT_NB_CPU_CTL_H1_0 HT_NB_CPU_CTL_H1_0 5
HT_NB_CPU_CTL_L1_0 HT_NB_CPU_CTL_L1_0 5



Close to U23



All external components connected to
SPMEM signals must be removed
for RX780



> +1.1V 10,12,13,37



PROJECT : TT9
Quanta Computer Inc.

Size B	Document Number RS780M-PCIE I/F 2/4	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 11 of 41

Enables the Test Debug Bus using GPIO.

0 : Enable
1 : Disable
(RS780 use VSYNC#)



Enables Side port memory

0 : Enable (RS780)
1 : Disable (RS780)
(RS780 use HSYNC#)



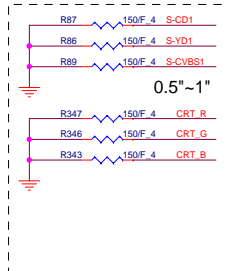
default values if not connected
RS780:SUS_STAT



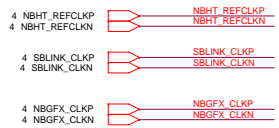
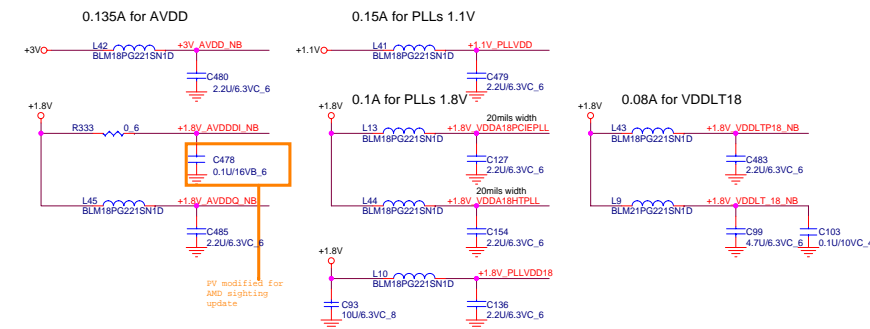
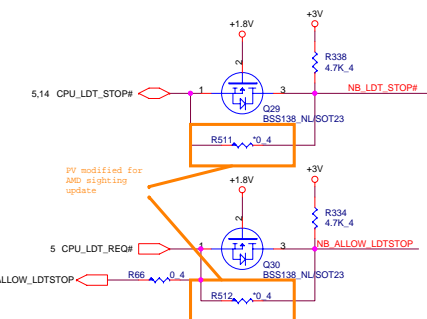
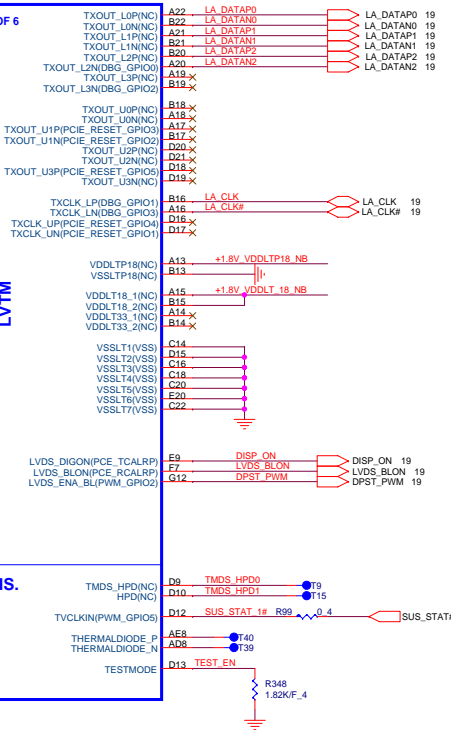
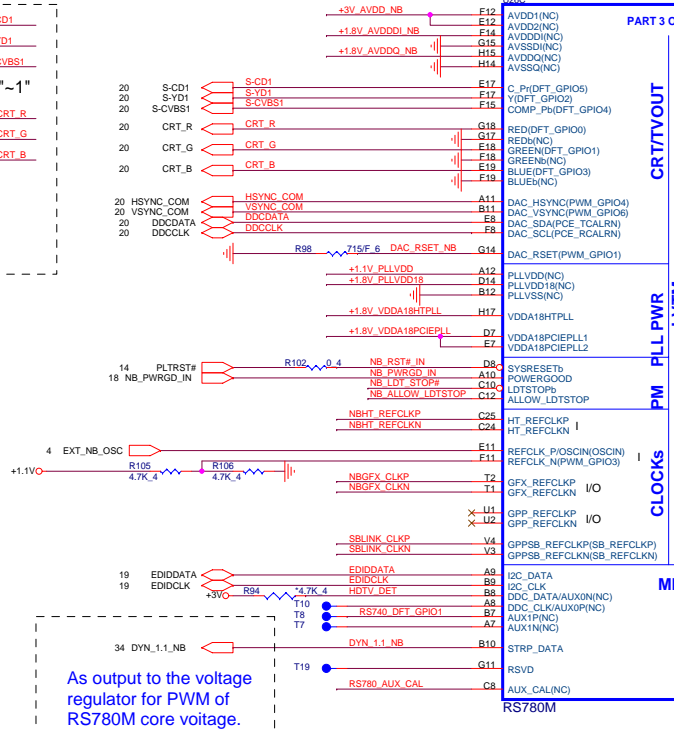
AUX CAL Value need update



PV modified for
AMD sighting
update

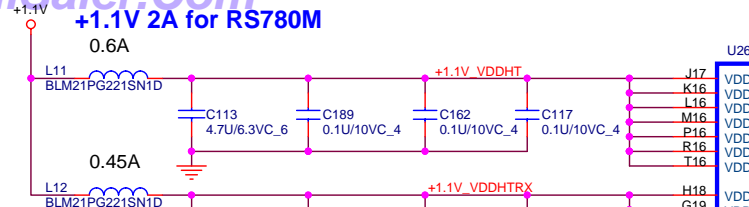


As output to the voltage
regulator for PWM of
RS780M core voltage.

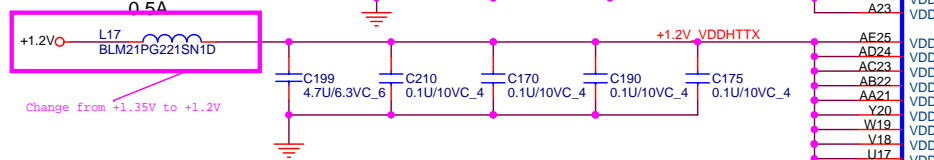


+1.1V 10,11,13,37
+1.8V 5,10,13,14,15,18,36,38
+3V 4,5,7,8,9,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38
+12VALW 19,28,31,33,38

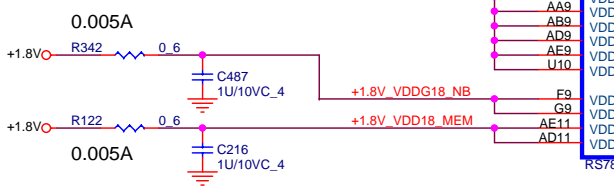
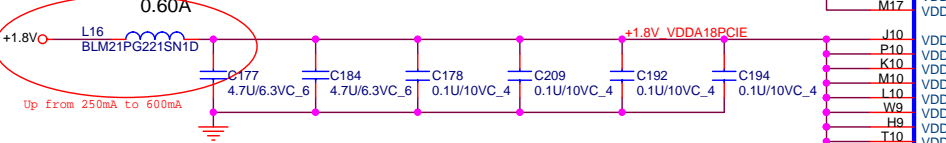
+1.1V 2A for RS780M



+1.2V 2A for RS780M+SB700

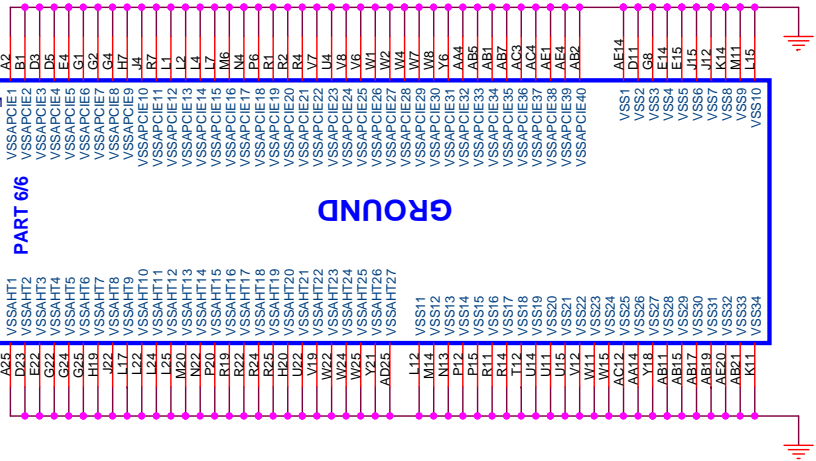
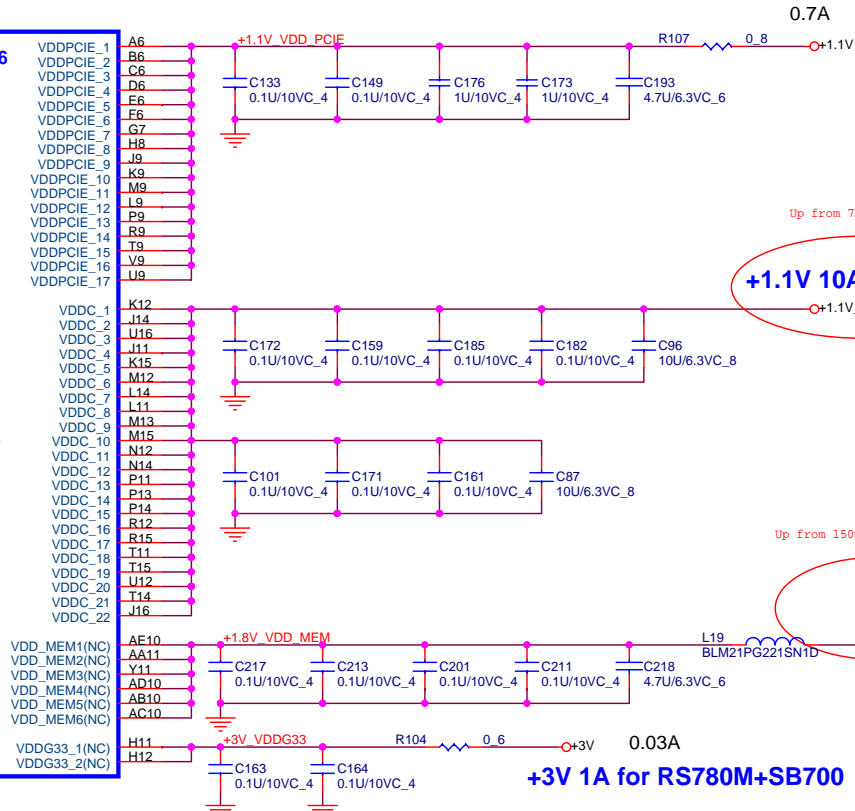


+1.8V 1A for RS780M+SB700



PART 5/6

POWER



GROUND

PART 6/6

- +1.1V NB 34
- +1.1V 10,11,12,37
- +1.2V 4,5,14,16,17,34,37
- +1.8V 5,10,12,14,15,18,36,38
- +3V 4,5,7,8,9,12,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38



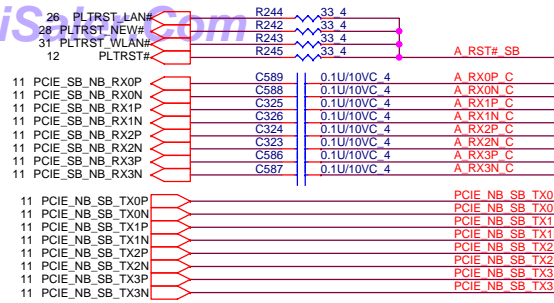
PROJECT : TT9
Quanta Computer Inc.

Size B	Document Number RS780M-POWER 4/4	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 13 of 41	

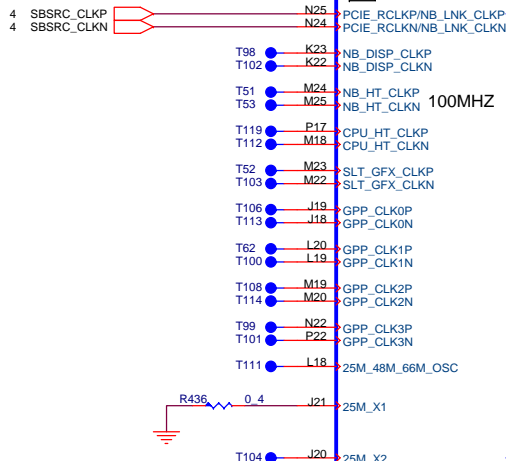
PLACE THESE
PCIe AC
COUPLING CAPS
CLOSE TO U600



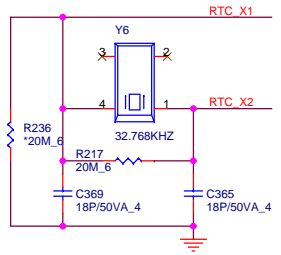
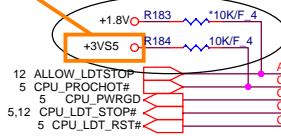
To RS780



1. PCIe Reference Clk (Ext Clk Gen)
2. A-link Clk to North Bridge (Int Clk Gen)



PV fix +3VSS leakage to +3V



Part 1 of 5

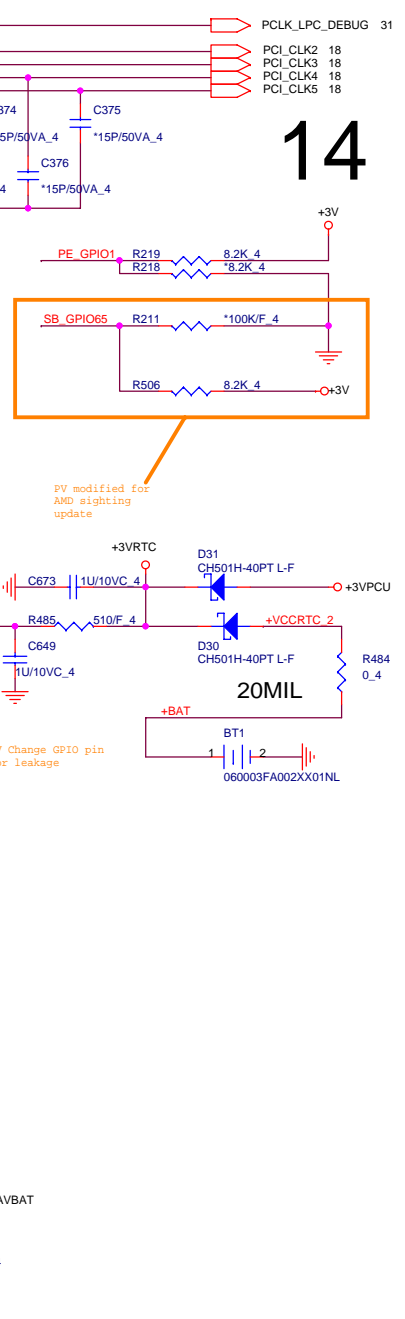
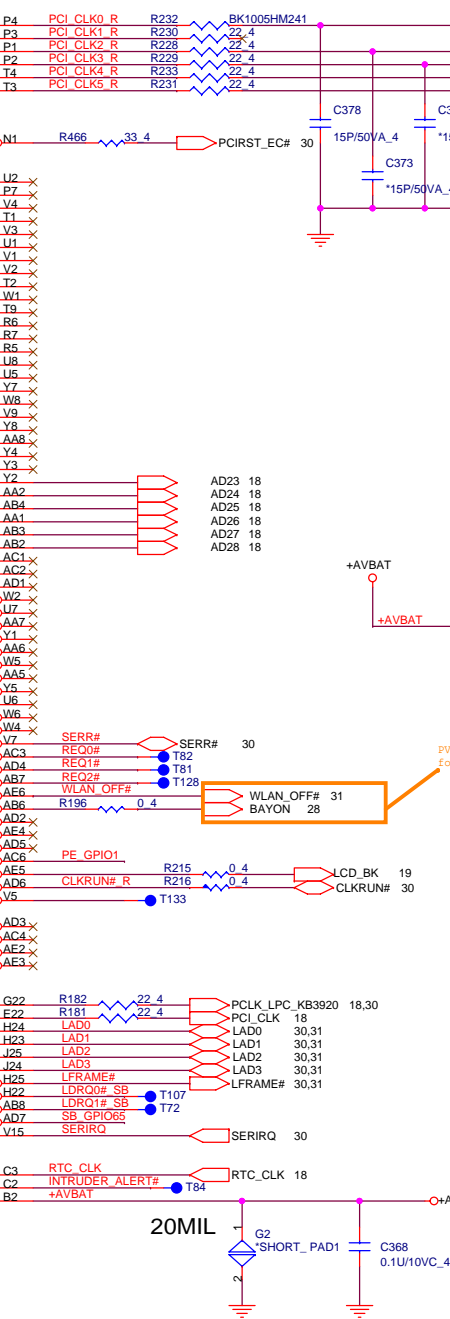
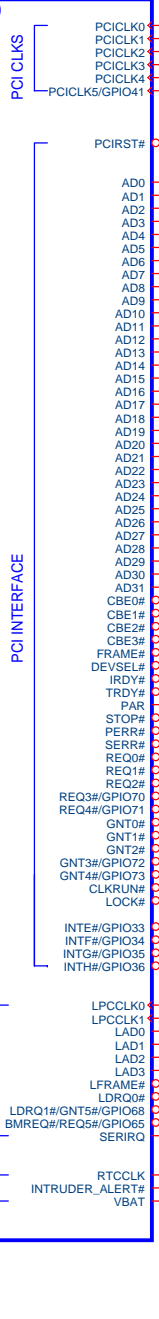
PCI EXPRESS INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

RTC



14

PV modified for
AMD sighting
update

PV Change GPIO pin
for leakage



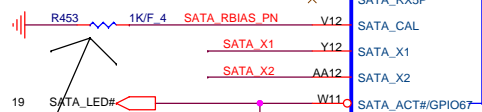
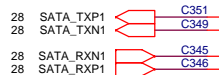
PROJECT : TT9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-PCIe/PCI/CPU/LPC 1/4	1A
Date: Wednesday, January 23, 2008	Sheet 14 of 41	

SATA1

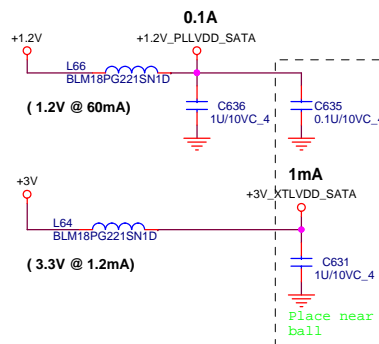
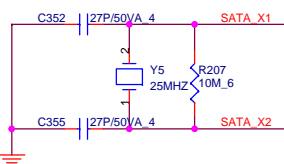


SATA ODD



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:
R635 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



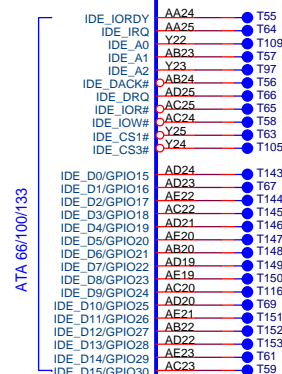
U16B

SB700
Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR

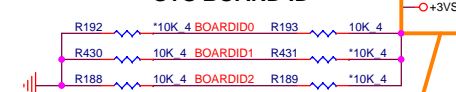


IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

VRAM / Clock Gen	Samsung Realtek (0.0.0)	Qimonda ICS (1.0.0)	Hynix Silego (0.1.0)
BOARDID0	R192 Stuff	R193 Stuff	R192 Stuff
BOARDID1	R430 Stuff	R430 Stuff	R431 Stuff
BOARDID2	R188 Stuff	R188 Stuff	R188 Stuff

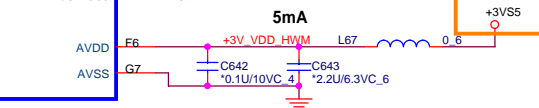
DB2 MODIFY

SYS BOARD ID



PV SB internal pull
Hi to 3V5S, modified
to samepower rail
with SB

PV fix +3V5S leakage to +3V



+1.2V 4,5,13,14,17,34,37
+3V 4,5,7,8,9,12,13,14,15,17,18,19,20,22,23,26,28,29,30,31,33,34,38

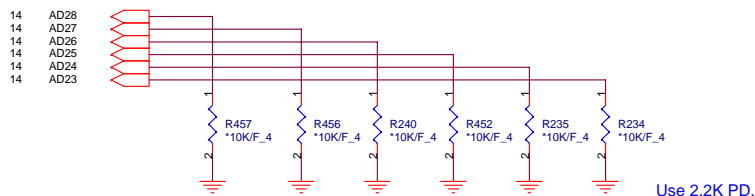


REQUIRED STRAPS

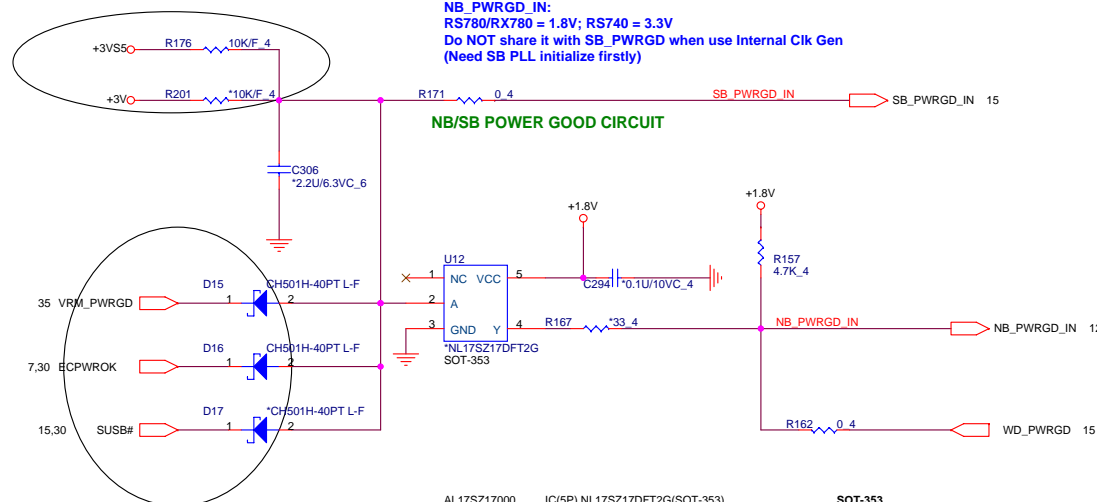
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCLK_LPC_KB3920	PCI_CLK	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM	DEFAULT

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



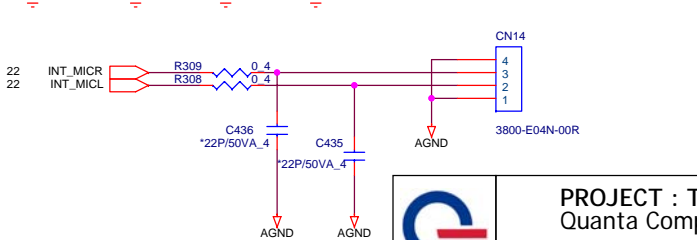
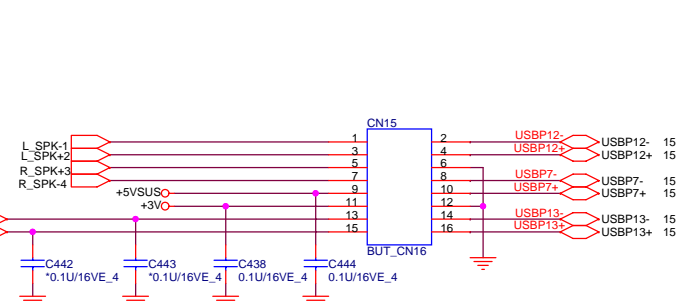
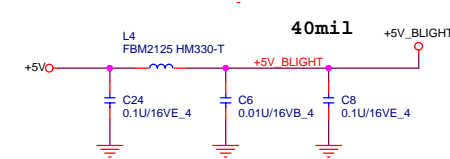
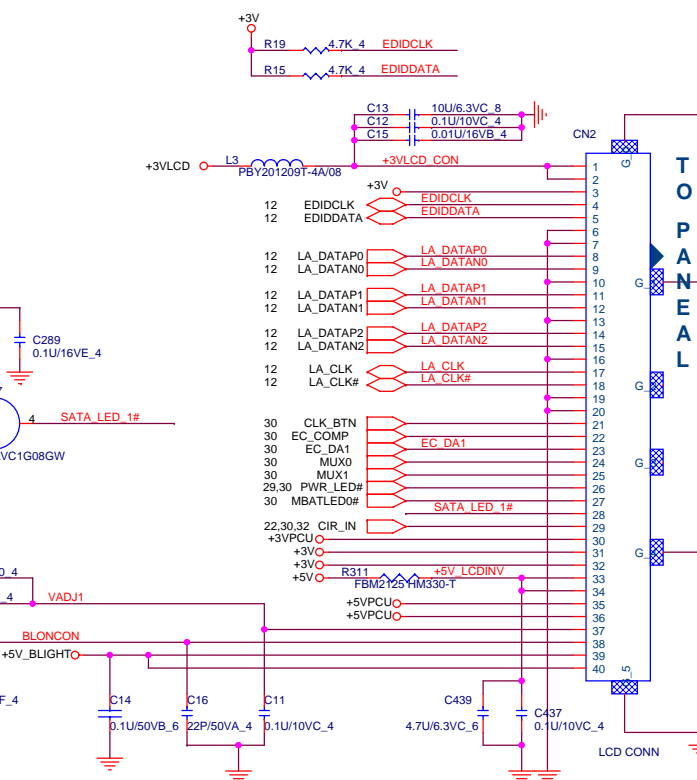
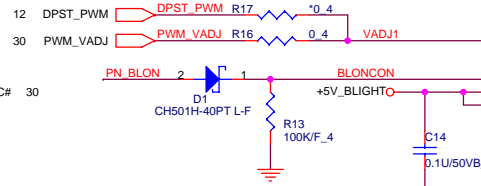
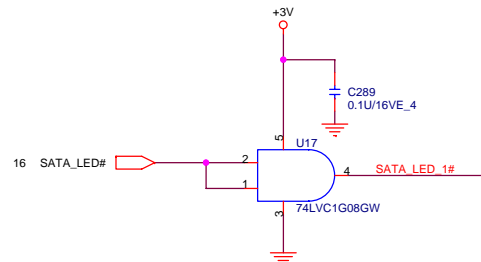
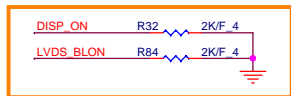
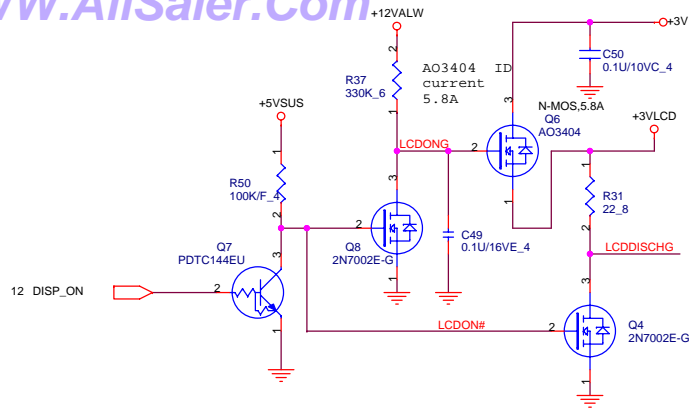
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : TT9
Quanta Computer Inc.

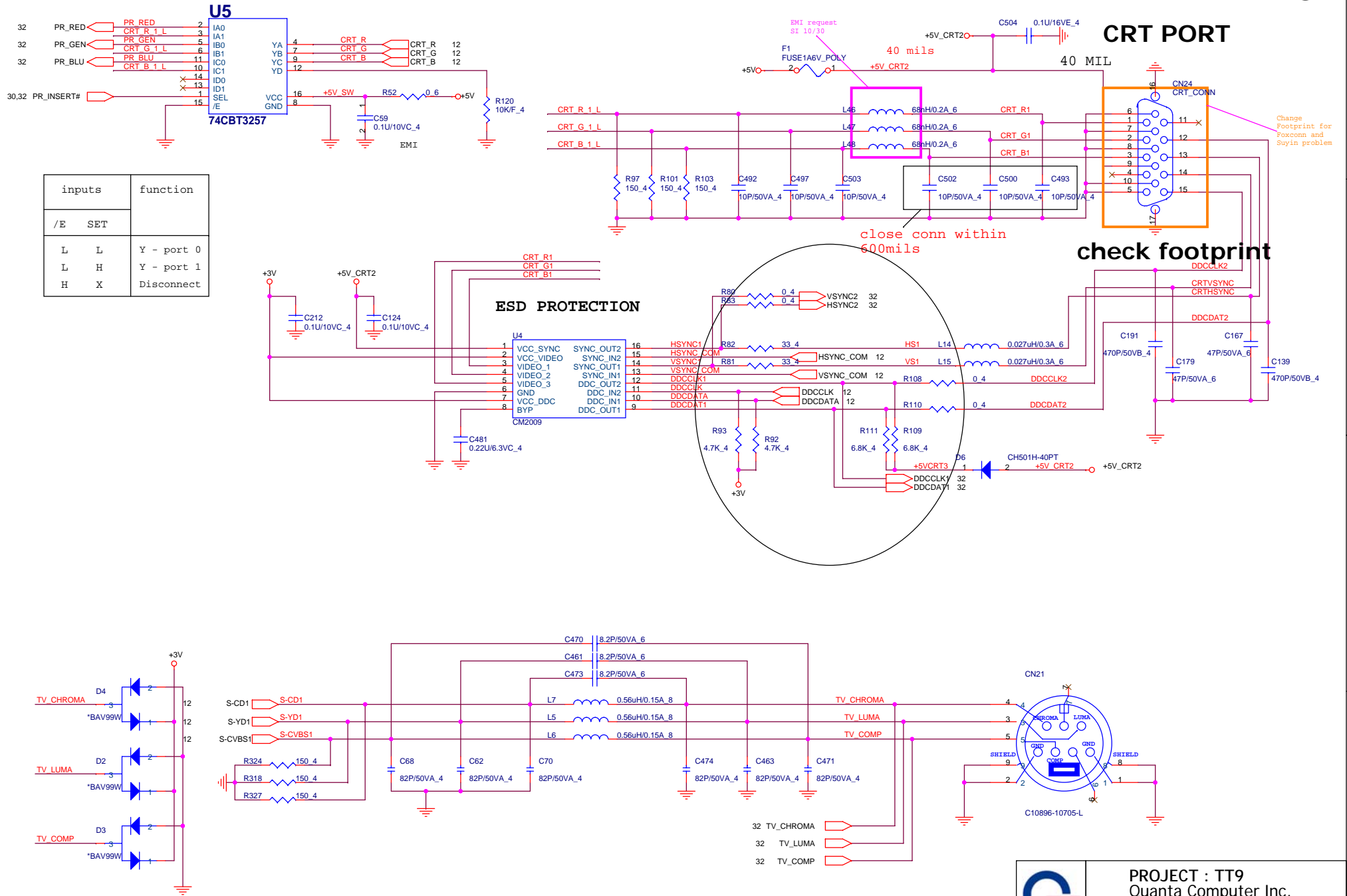
Size Custom	Document Number SB700-STRAPS,PWRGD	Rev 1A
Date: Wednesday January 23, 2008 Sheet 18 of 41		



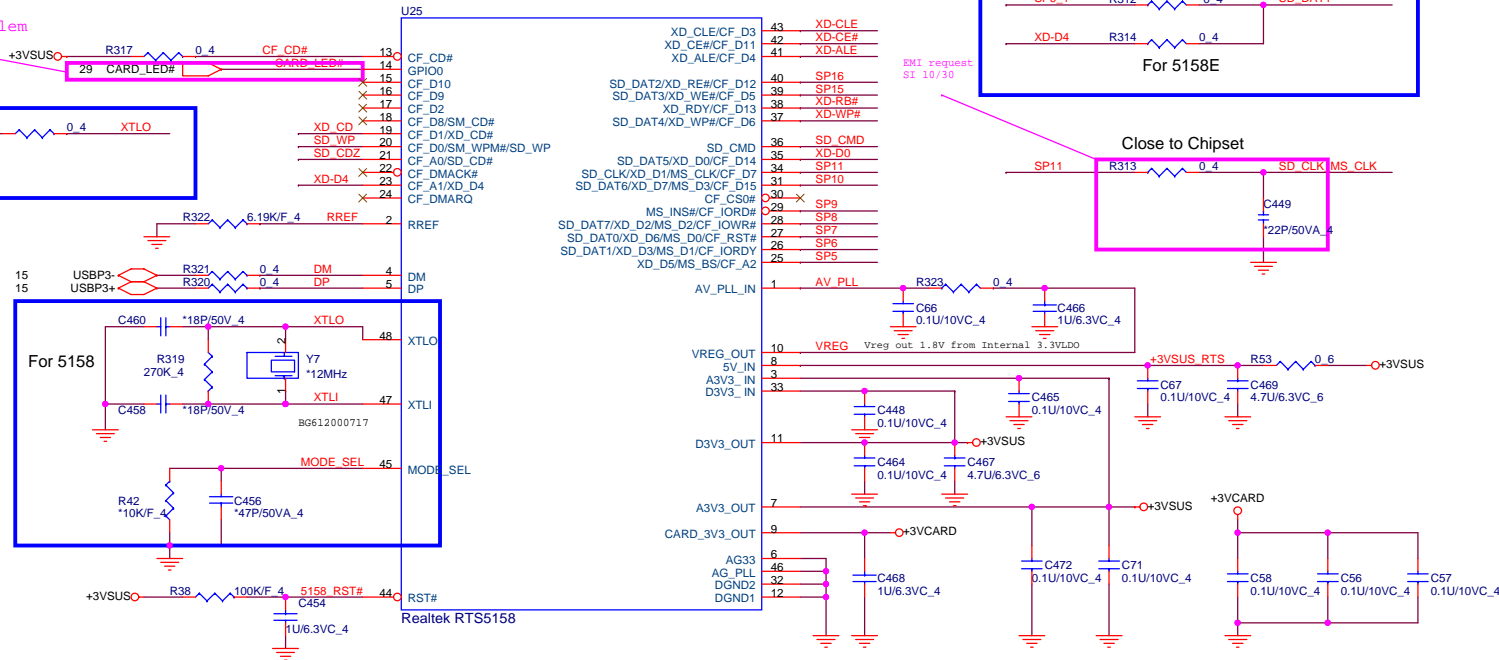
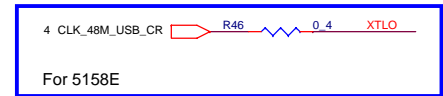
Finger Printer
Camera
Digitizer

+3VPCU 5,14,25,29,30,32,33,35,37,39
+3V 4,5,7,8,9,12,13,14,15,16,17,18,20,22,23,26,28,29,30,31,33,34,38
+3VSUS 15,21,24,25,29,31,33,34,35,36,38
+5V 17,20,22,23,28,31,32,33,37,38,39
+12VALW 28,31,33,38

Speaker
+5VSUS --> Camera
+3V --> FP/Digitizer
Digitizer control signal



	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4			XD D4
SP5		MS BS	XD D5
		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT1	MS D2	XD D7
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D2
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

[illegible]

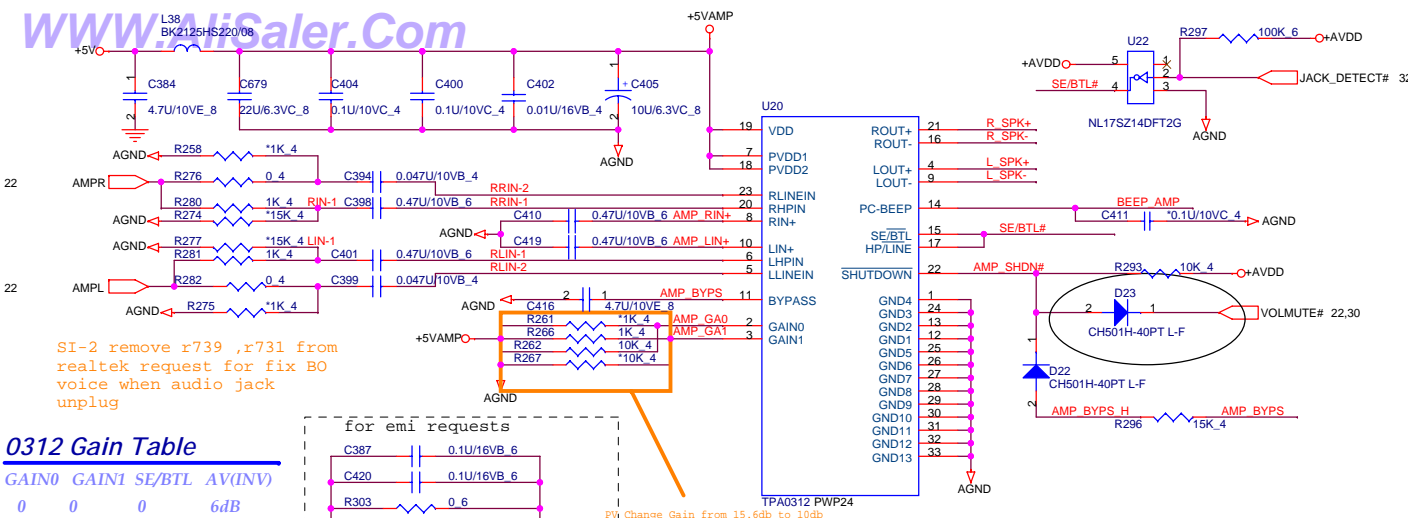
Pinout diagram for the CM4M-025 module. The module is a rectangular component with pins numbered 1 to 39. It has two 3V3CARD power pins at the top (pins 1 and 39). The left side has pins for RD-RB#, SP16_1, XD-CE#, XD-CLE#, XD-ALE#, SP15_1, XD-WP#, XD-D0, SP17_1, SP16_1, SP15_1, and SD_CMD. The right side has pins for SP7_1, SP6_1, SP5, SD_CLK, SD CLK, SP7_1, SP8_1, SP6_1, XD-D4, SD_DAT1, SP5, SP7_1, SP10_1, XD_CD, SD_WP, and SD_CDZ. The bottom has pins for GND1, GND2, GND3, and GND4. The module is labeled 'CN30' and 'CM4M-025'.

Remove Acce from HP information

PROJECT : TT9
Quanta Computer Inc.

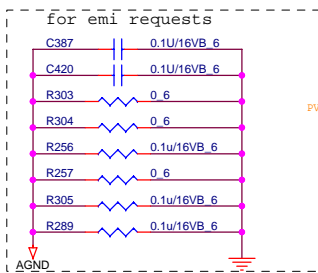


Size Custom	Document Number RT5158 CARD READER CONTROLLER	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 21 of 41

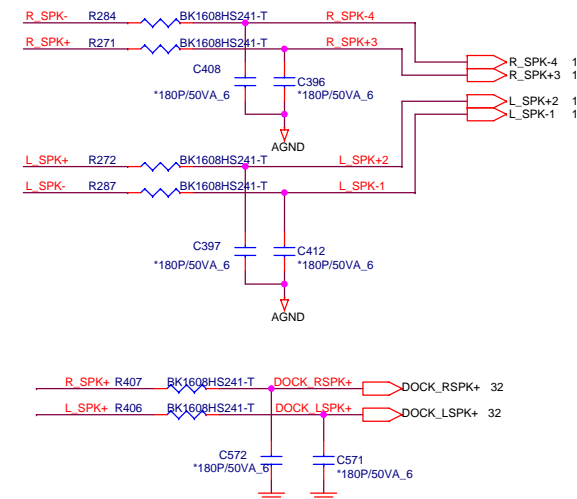


0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

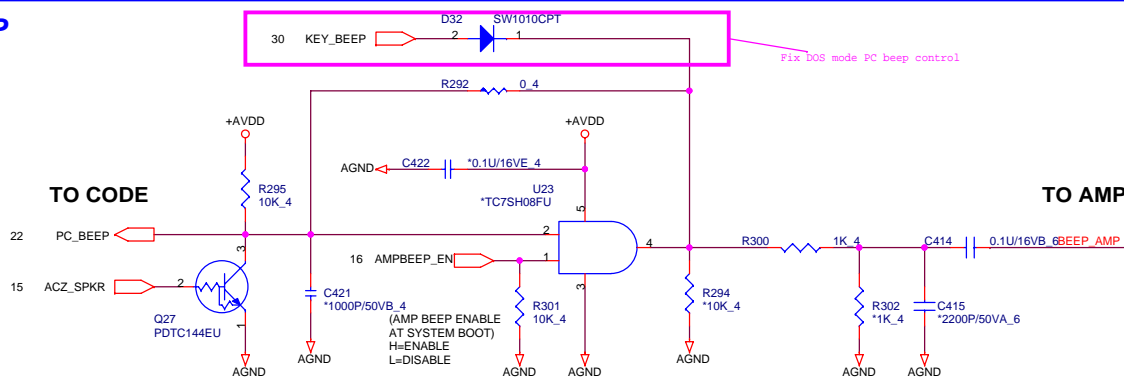


INT. SPEAKER

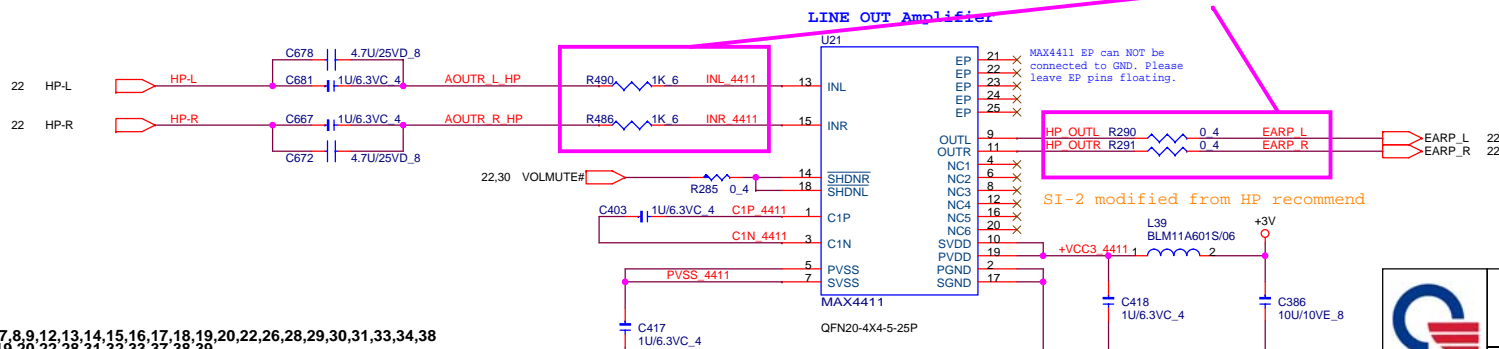


AUDIO AMPLIFIER

PCSPK BEEP



LINE OUT Amplifier

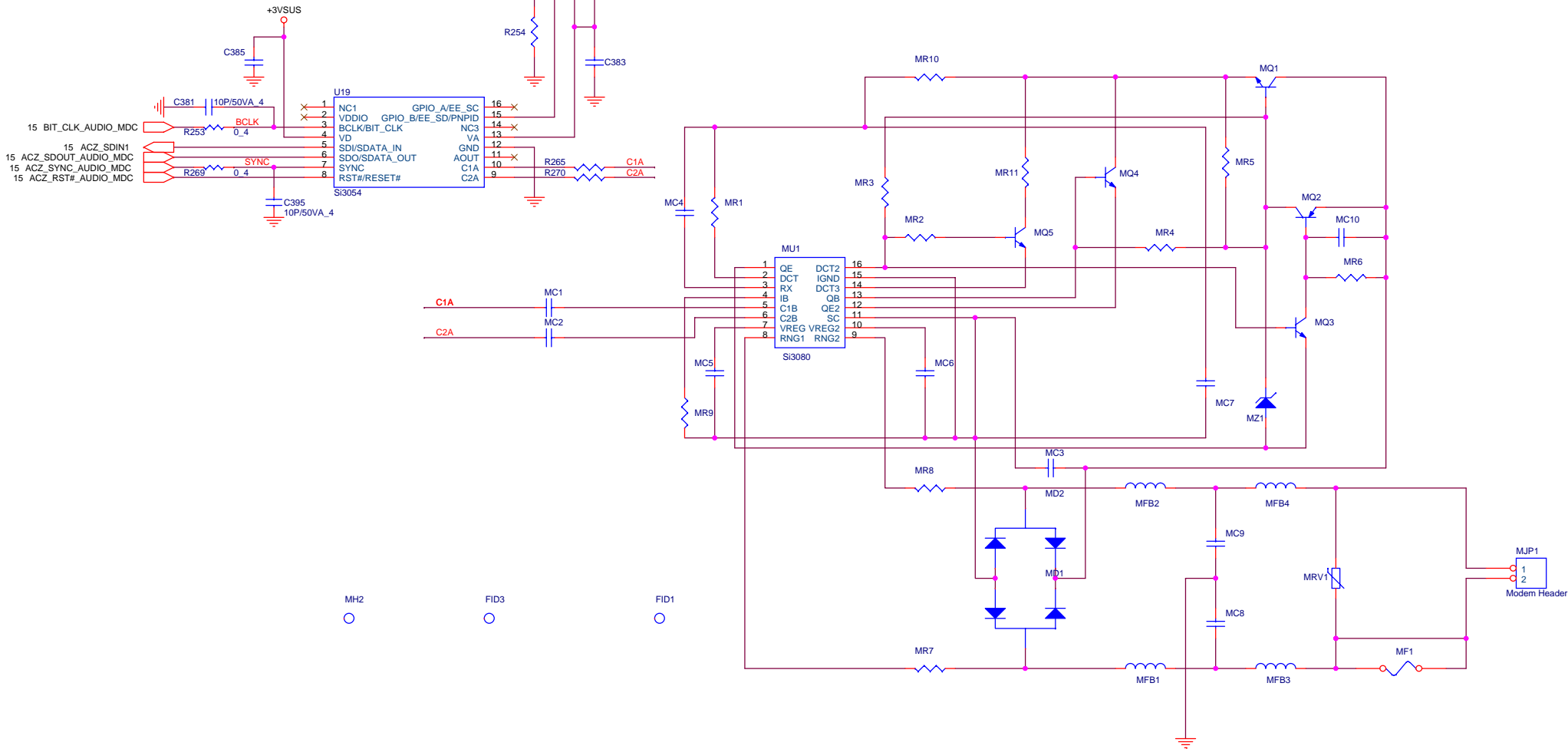


+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,26,28,29,30,31,33,34,38
 +5V 17,19,20,22,28,31,32,33,37,38,39
 +AVDD 22



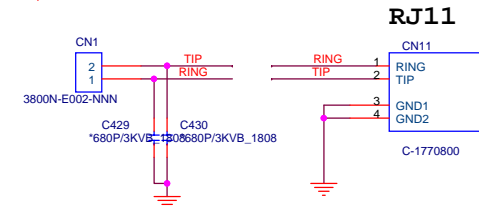
PROJECT : TT9
Quanta Computer Inc.

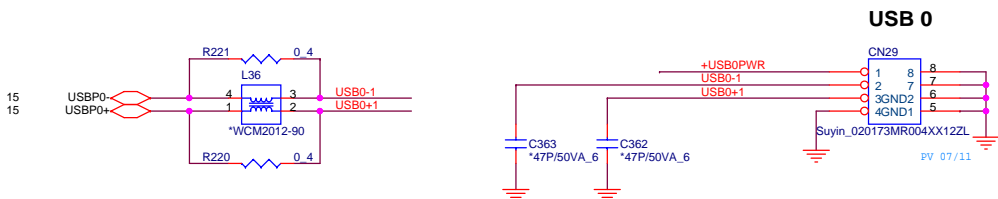
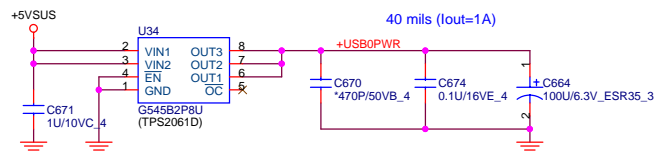
Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 23	of 41



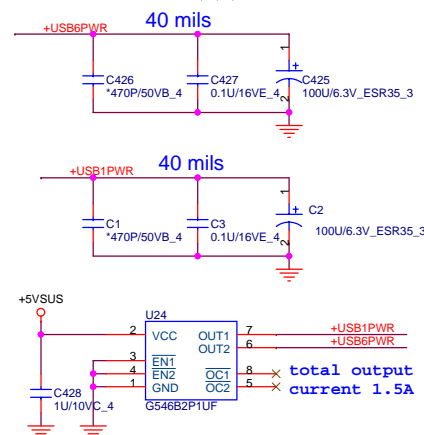
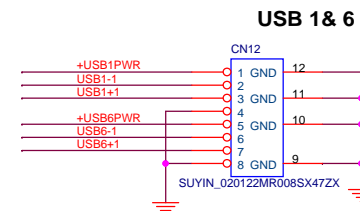
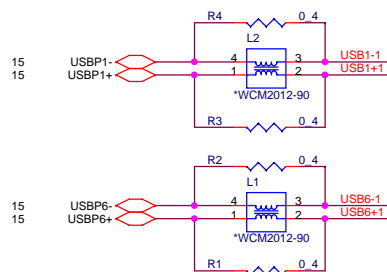
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

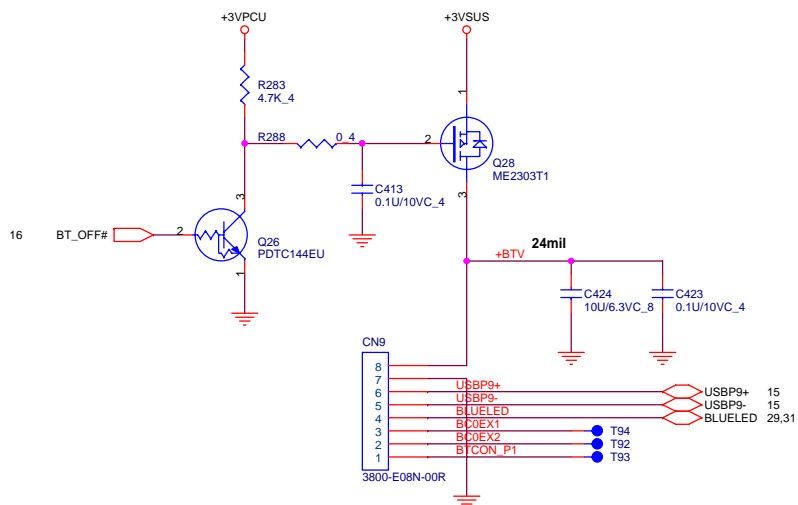




USBX2

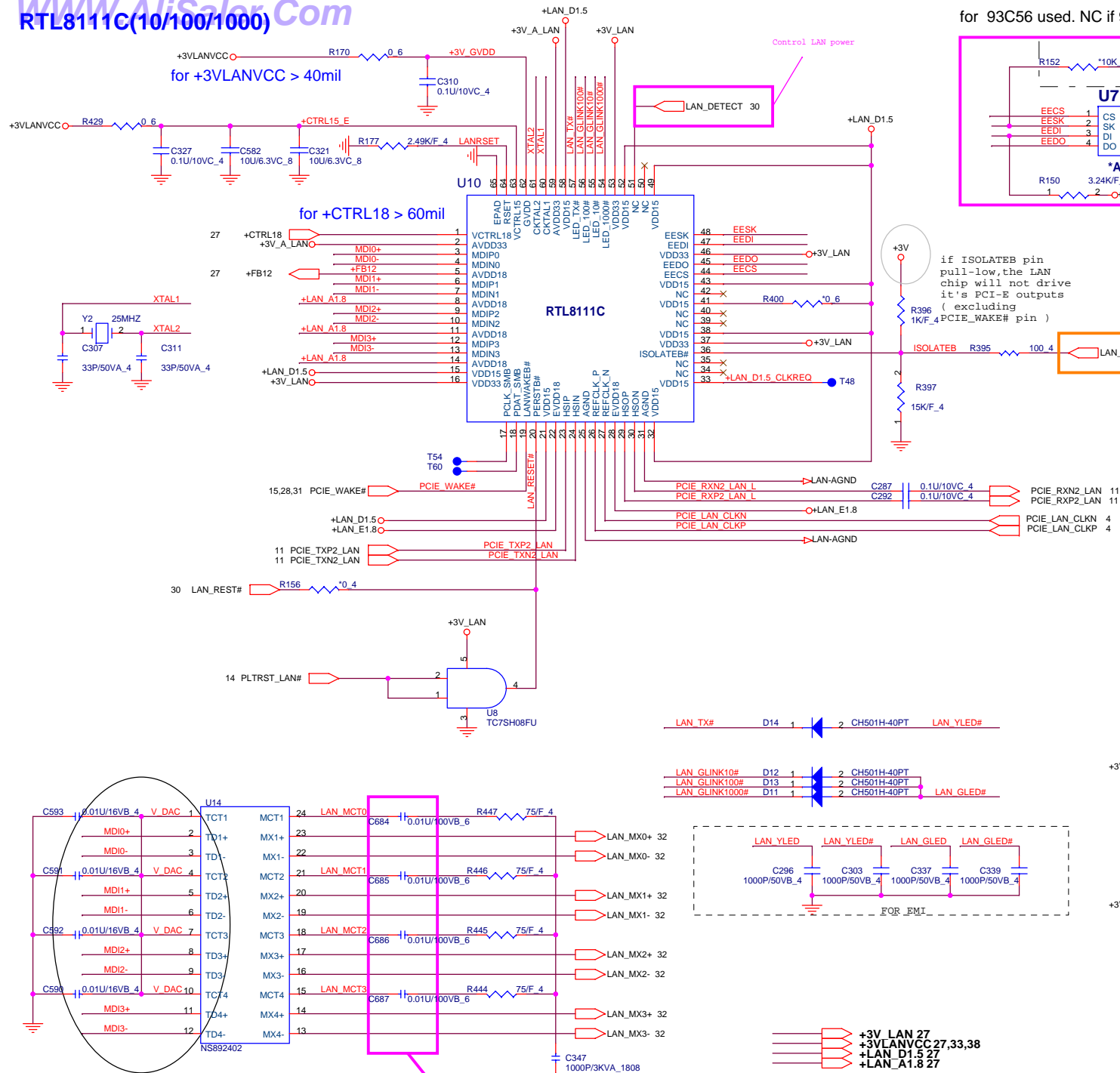


BLUETOOTH



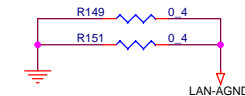
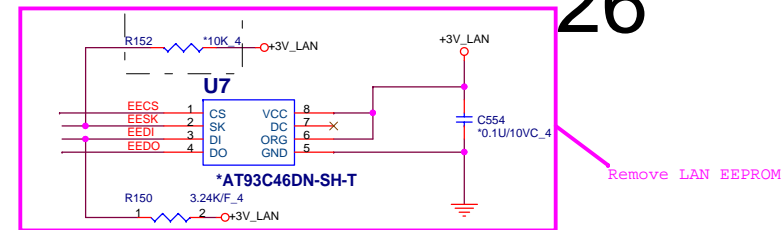
Select TPM function from HP information

+3VPCU 5,14,19,29,30,32,33,35,37,39
+3VSUS 15,21,24,29,31,33,34,35,36,38
+5VSUS 19,30,32,33,38



for 93C56 used. NC if 93C46 is used.

26

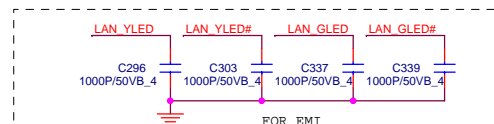
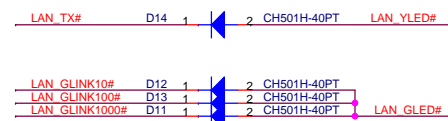


```
if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

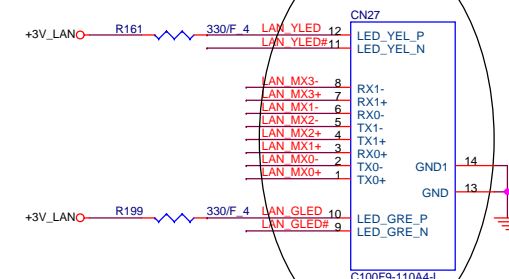
PV change from SB to EC control

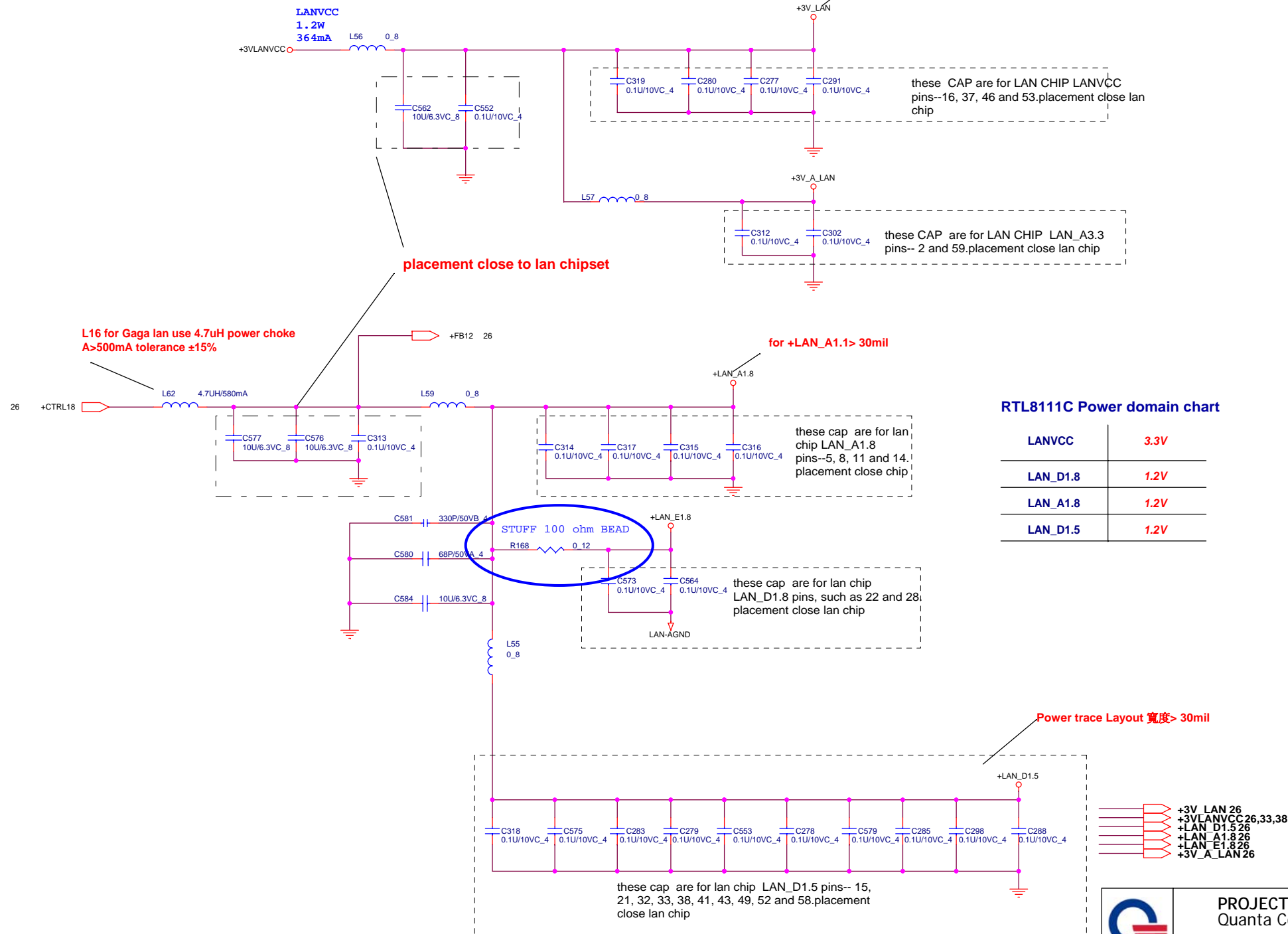


RJ45

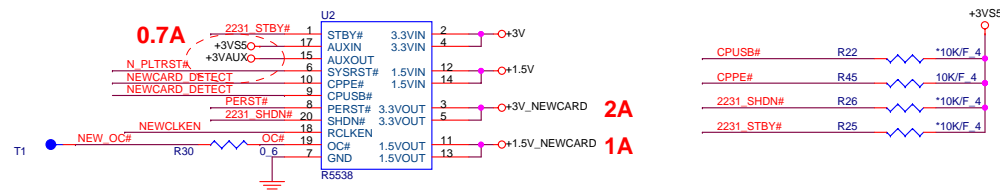
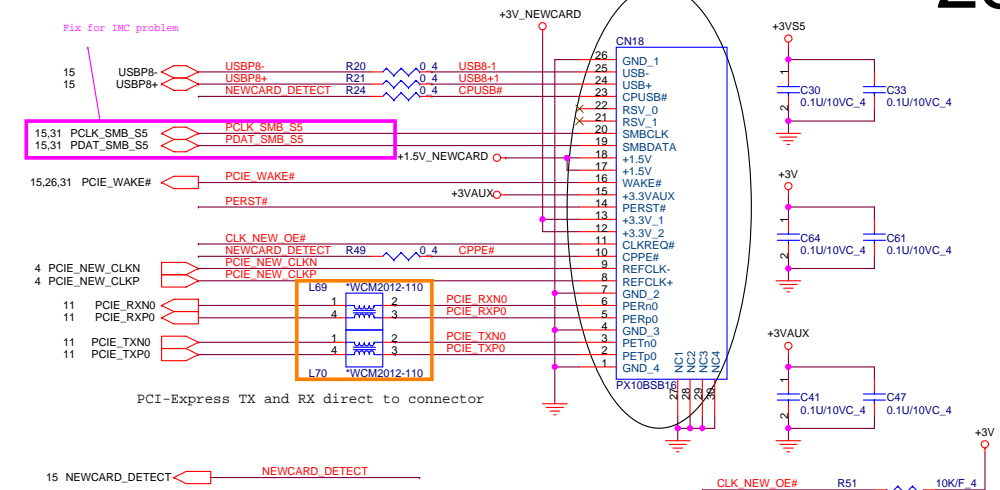


+3V LAN 27
+3VLANVCC 27,33,38
+LAN_D1.5 27
+LAN_A1.8 27

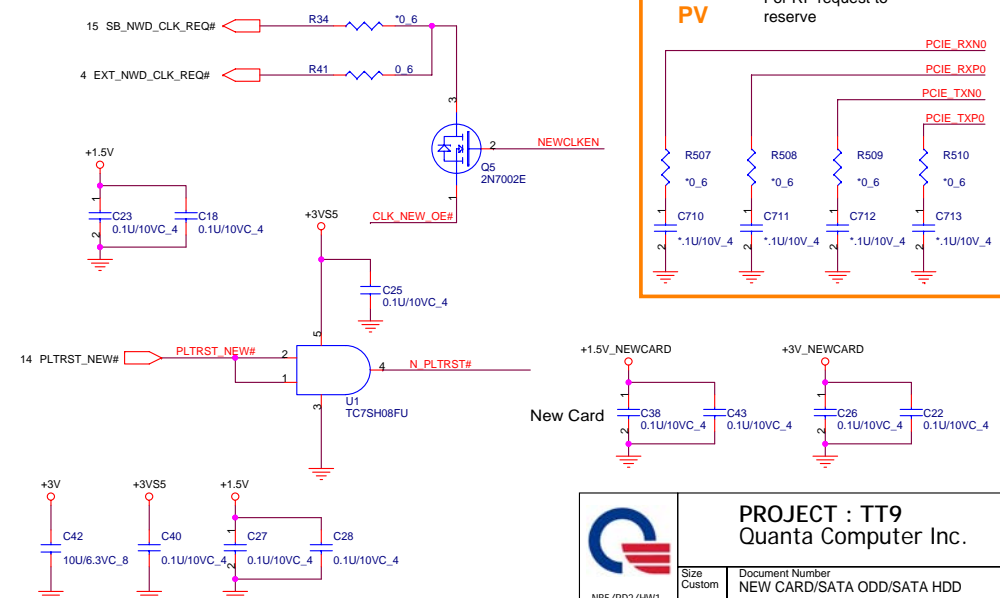




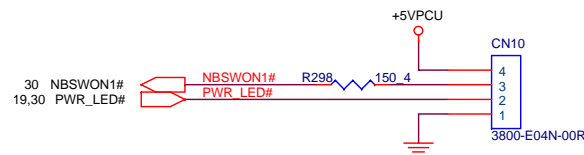
NEWCARD (PCIEXPRESS*1 + USB*1)



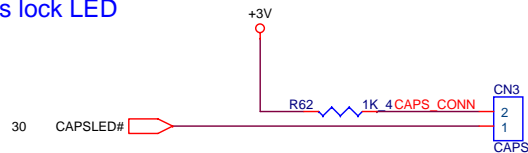
Change net name from 3V_NEWAUX to 3VAUX



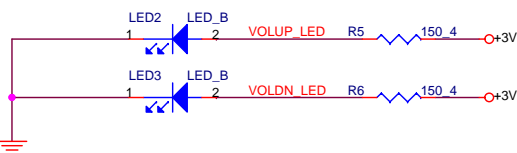
FOR POWER ON SW BOARD



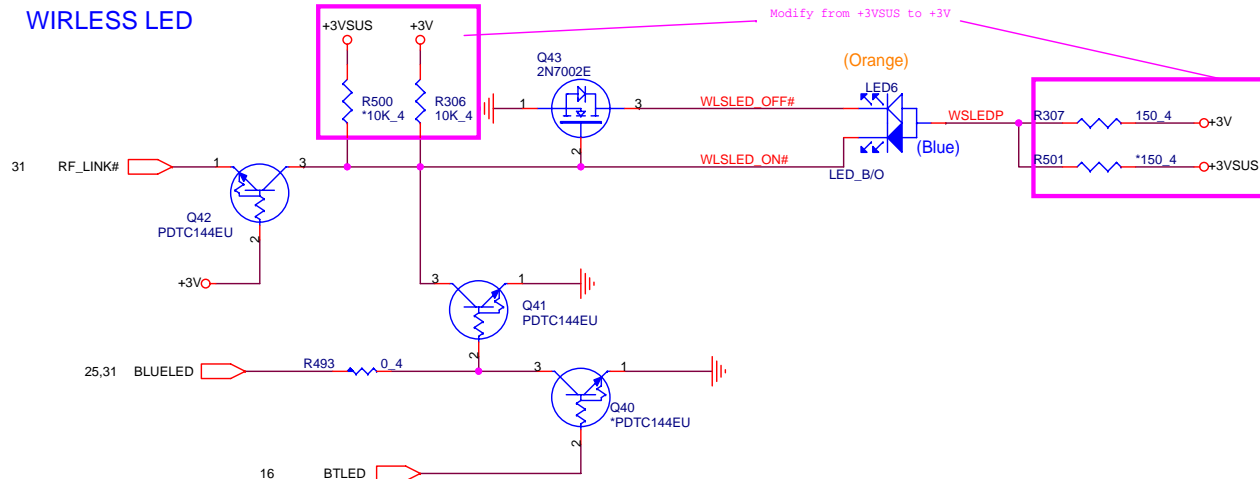
Caps lock LED



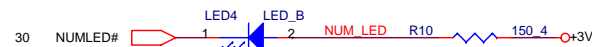
Volume up/down LED



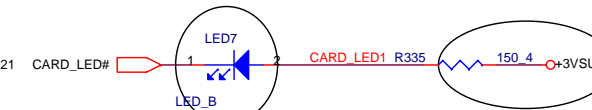
WIRLESS LED



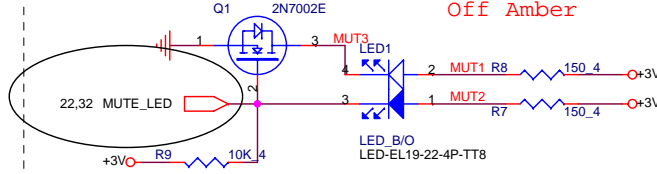
Num lock LED



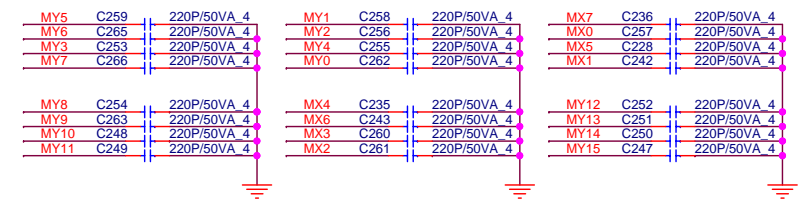
Card Reader LED



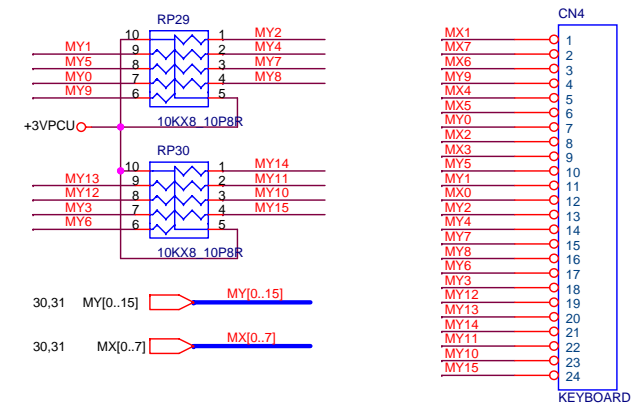
Mute LED



Keyboard



KEYBOARD PULL-UP

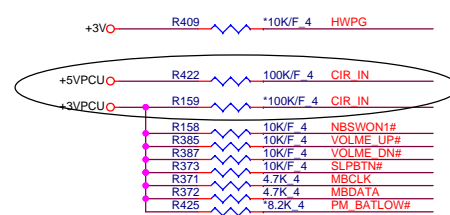
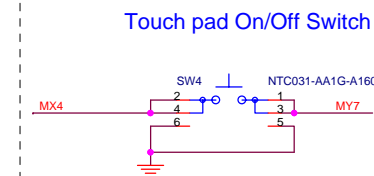
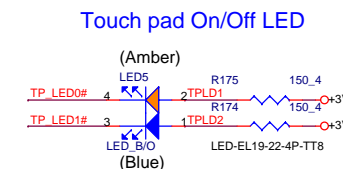
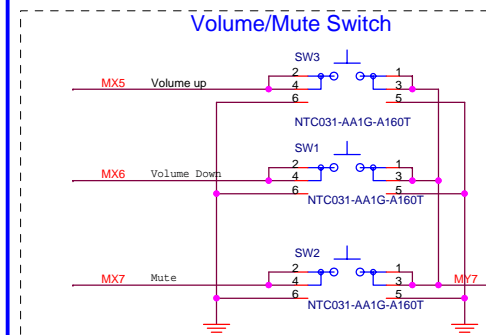
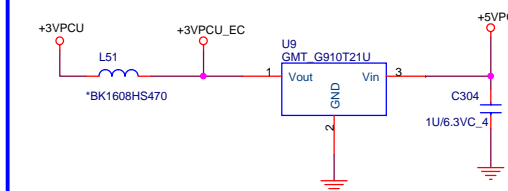
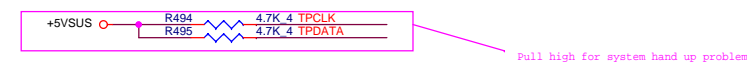
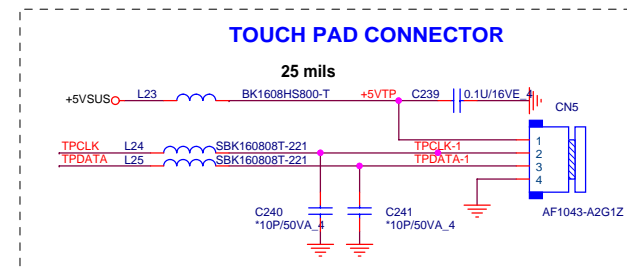


+5VPCU 19,22,28,30,33,34,35,36,37
+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38
+3VSUS 15,21,24,25,31,33,34,35,36,38

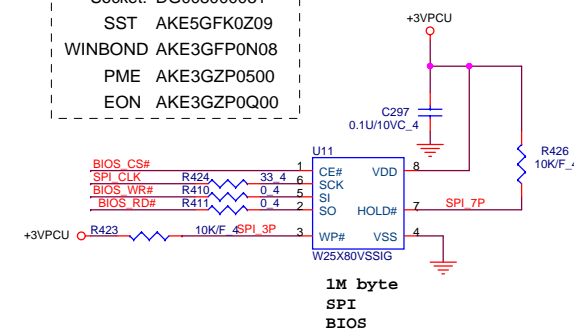


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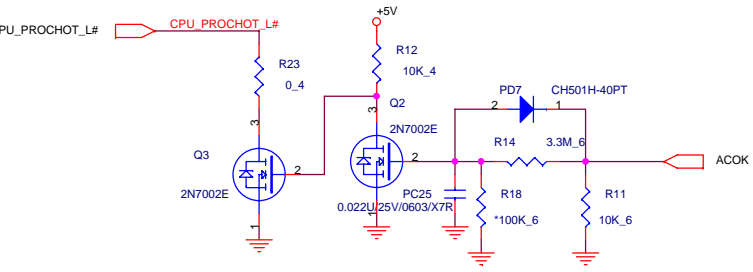
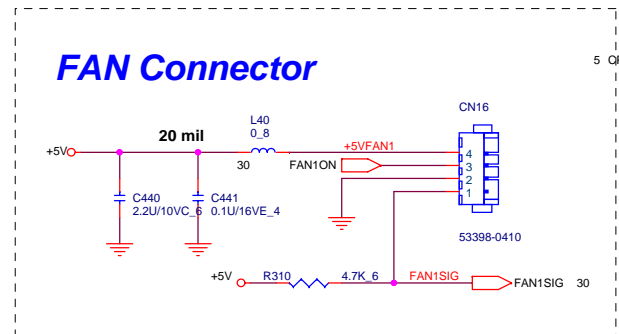
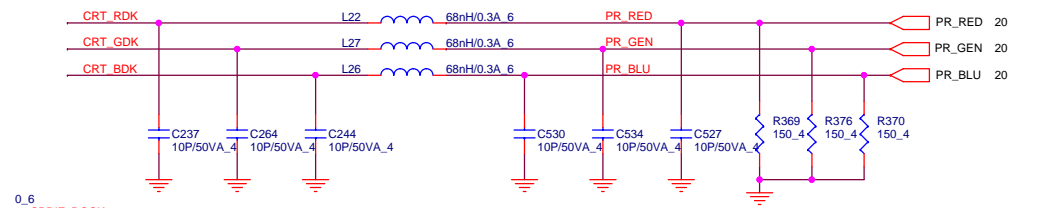
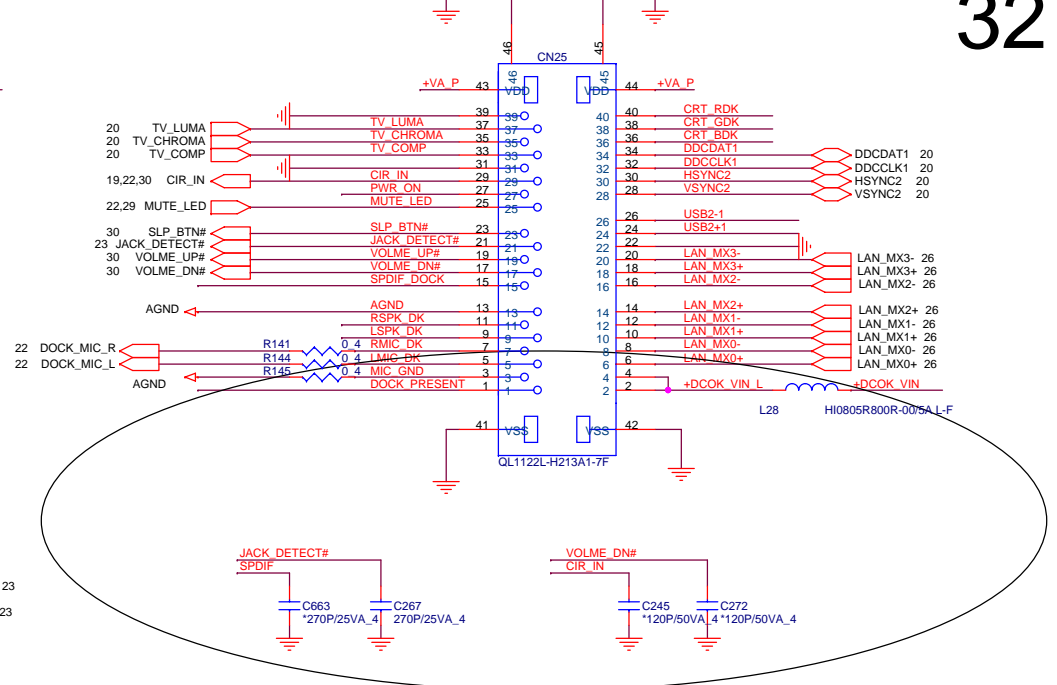
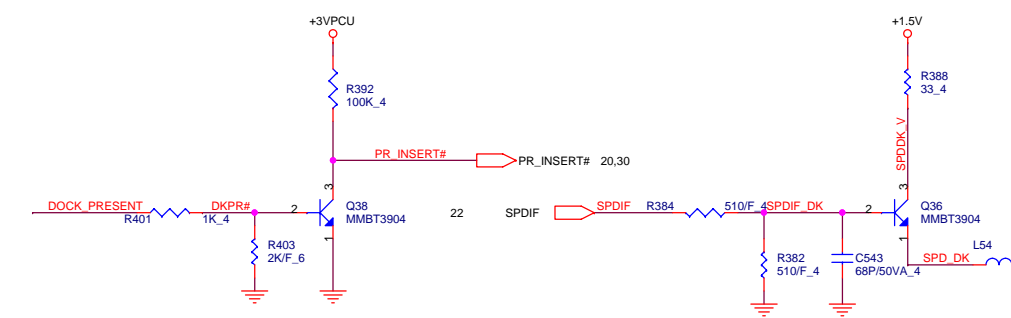
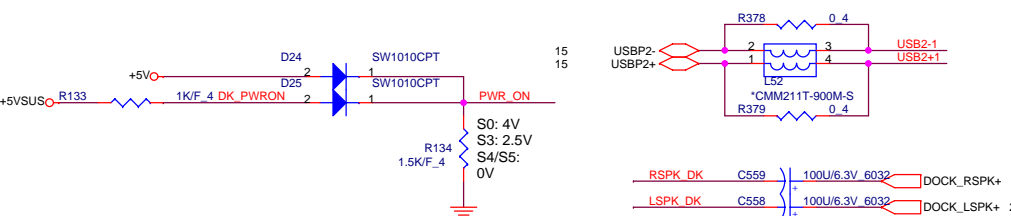
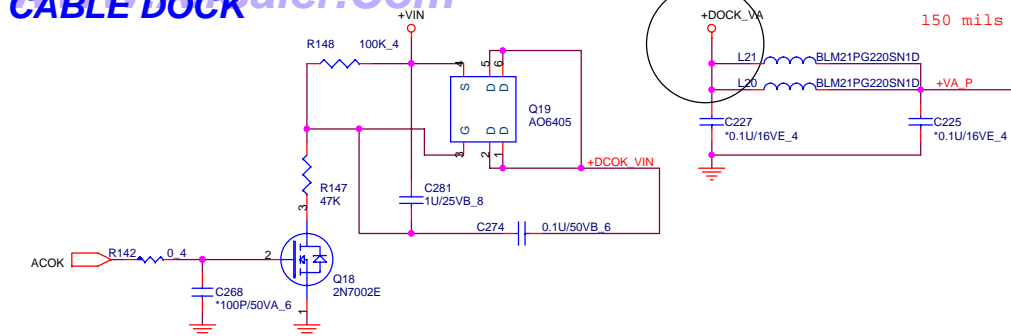
Size B	Document Number LED/KEYBOARD/SW	Rev 1A
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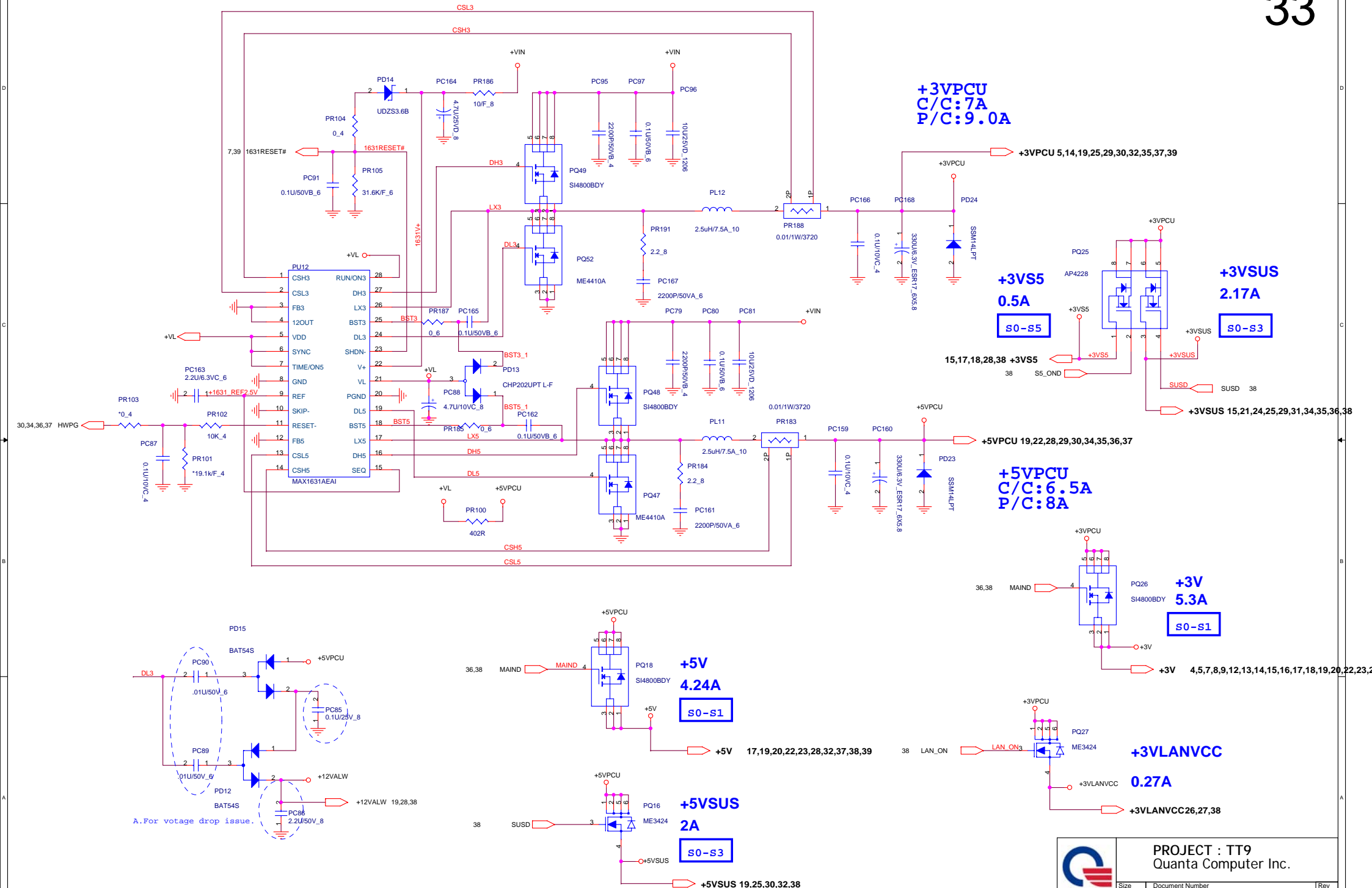
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WINBOND AKE3GFP0N08
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      EON AKE3GZP0Q00
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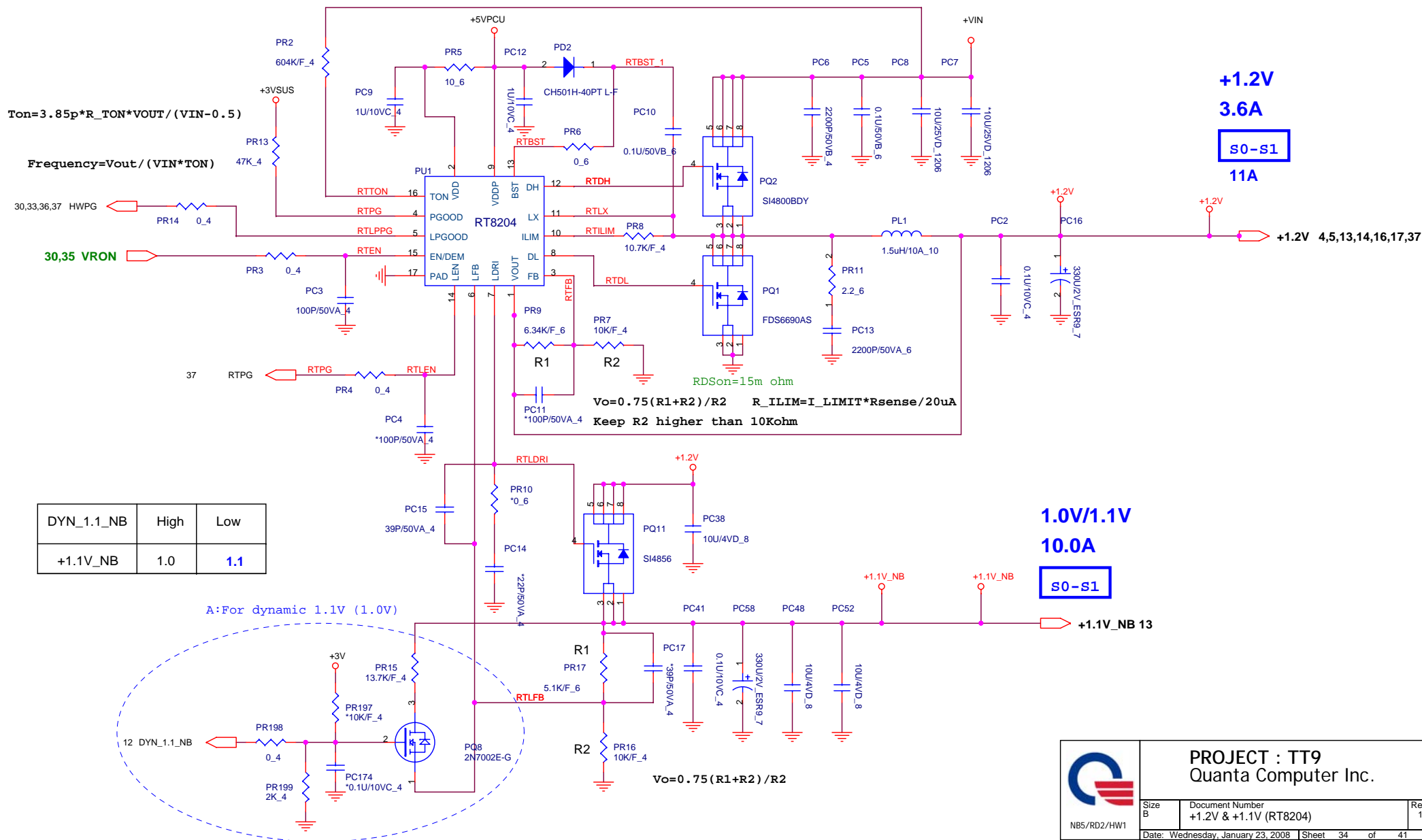


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- +5VSUS 19,25,30,33,38
- +5V 17,19,20,22,23,28,31,33,37,38,39
- +3VPCU 5,14,19,25,29,30,33,35,37,39
- +DOCK_VA 39
- +1.5V 28,31,37
- +VIN 31,33,34,35,36,38,39





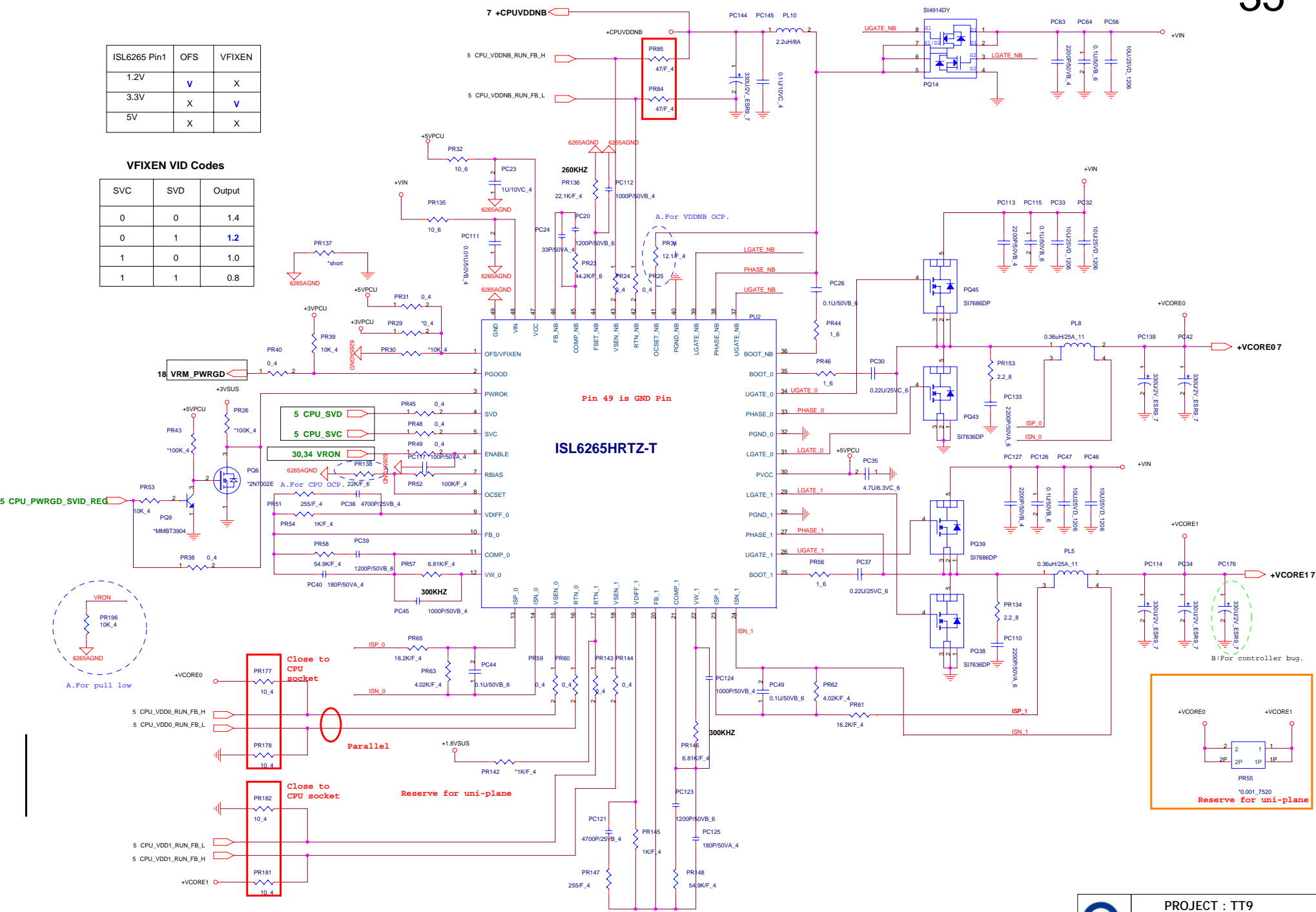
PROJECT : TT9
Quanta Computer Inc.

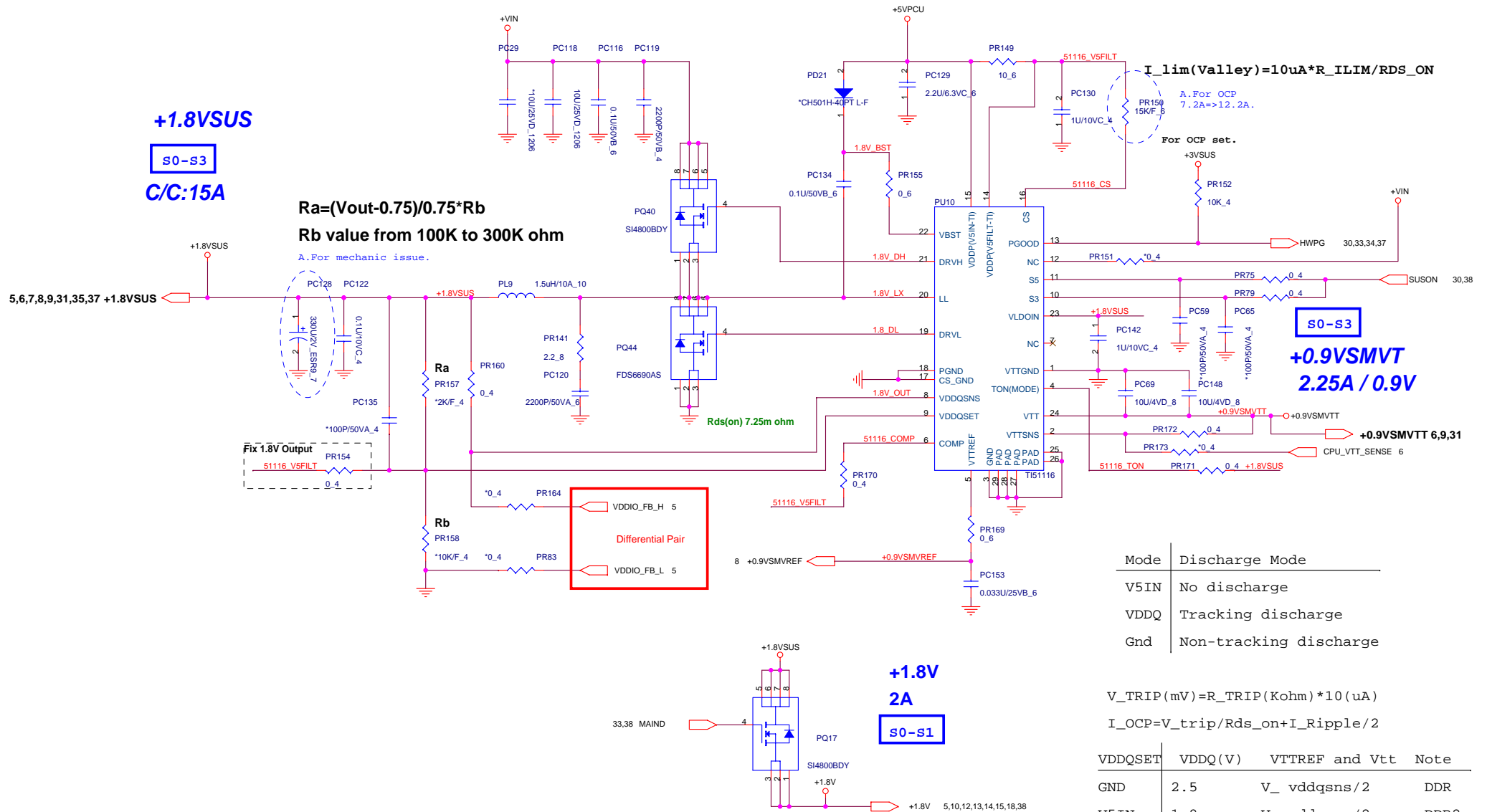
Size B	Document Number +1.2V & +1.1V (RT8204)	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 34	of 41

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

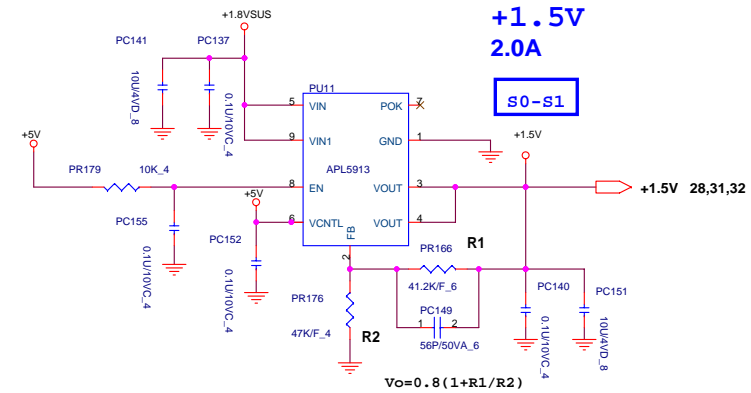
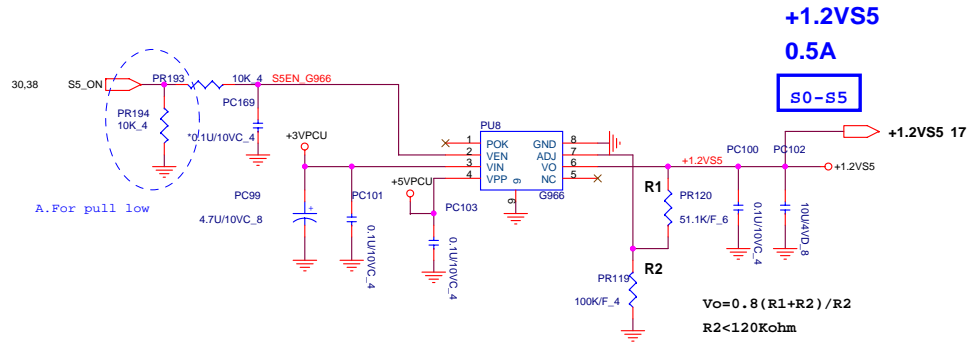
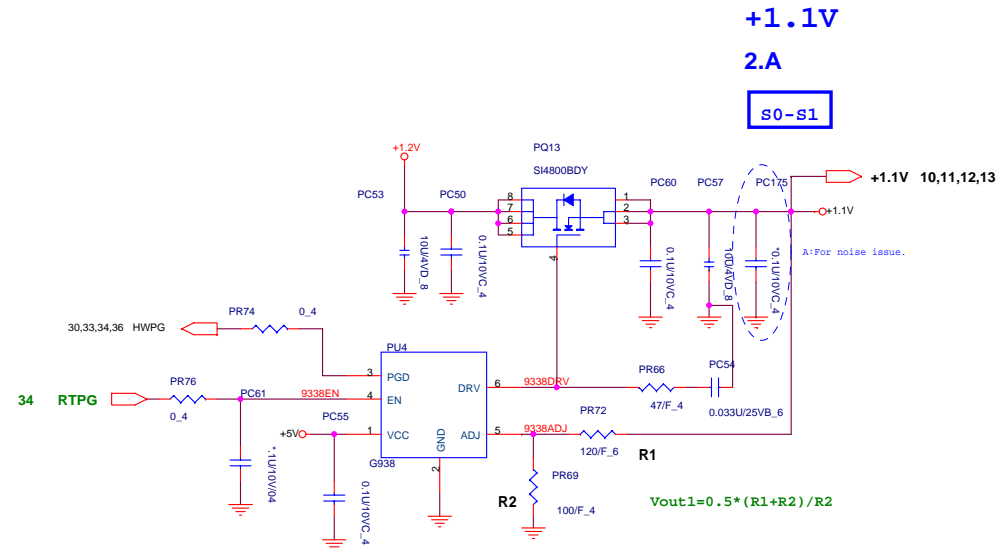
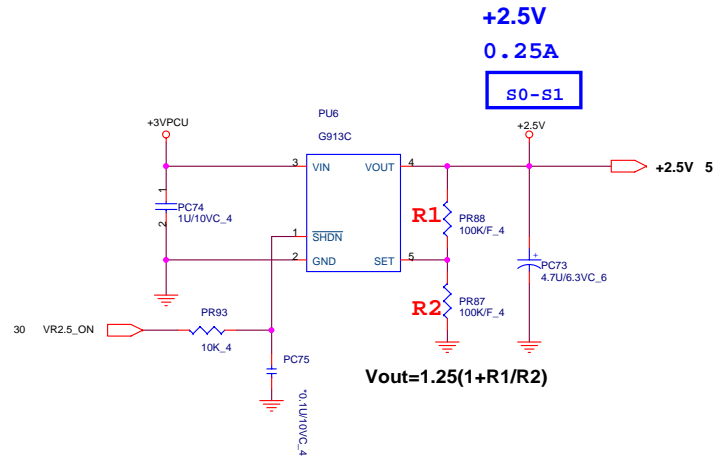
SVC	SVD	Output
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0	1	1.2
1	0	1.0
1	1	0.8




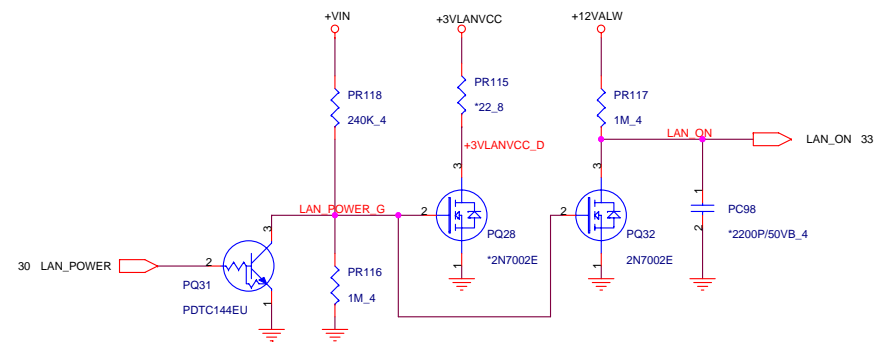
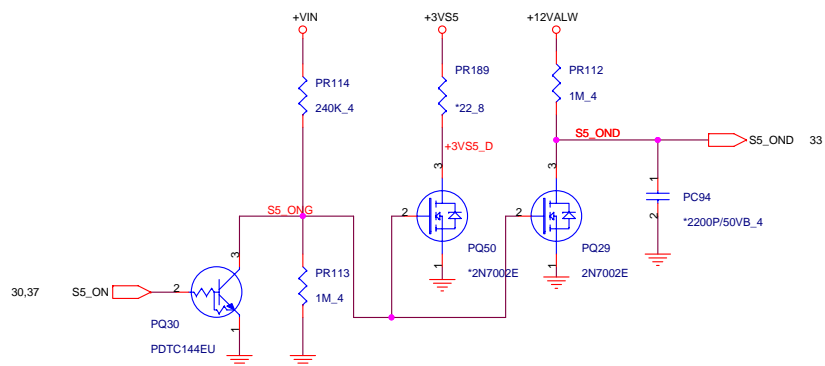
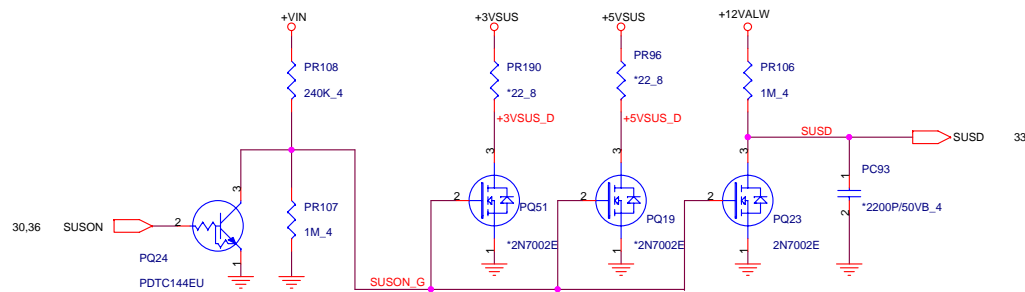
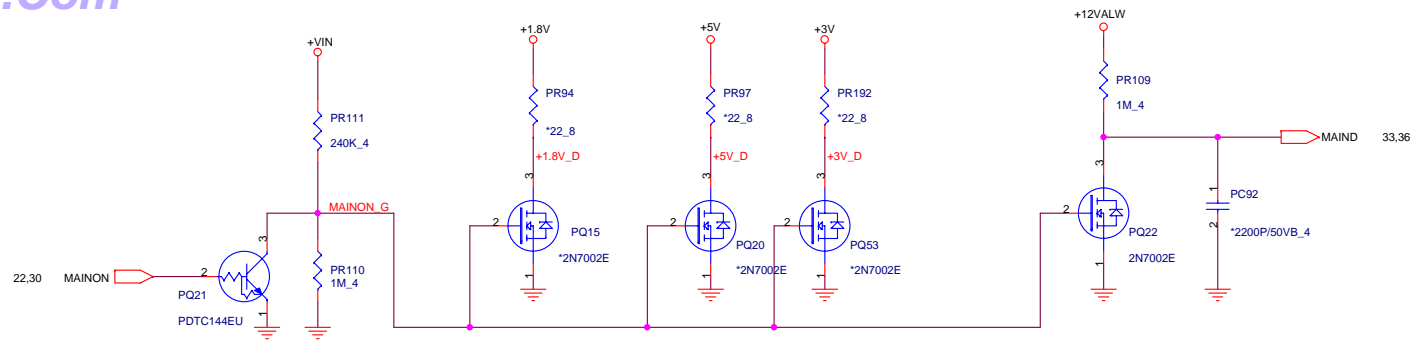



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Size Custom	Document Number 1.8VSUS/DDR_VTER/+1.8V/2.5V	Rev 1A
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Size Custom	Document Number +1.2V_S5/+1.5/+1.1V/+2.5V	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 37 of 41		



 NB5/RD2/HW1	PROJECT : TT9 Quanta Computer Inc.		
	Size Custom	Document Number DISCHARGE	Rev 1A
	Date: Wednesday, January 23, 2008	Sheet 38 of 41	

Charge current:
4 & 6 cell =>3A
8 cell =>3.5A

